Vivado-Instalacija programa

Instalacija je dostupna za slobodno preuzimanje sa sledećeg linka:
https://www.xilinx.com/support/download.html

Napomena:
Vivado ne podržava 32-bitne procesore.

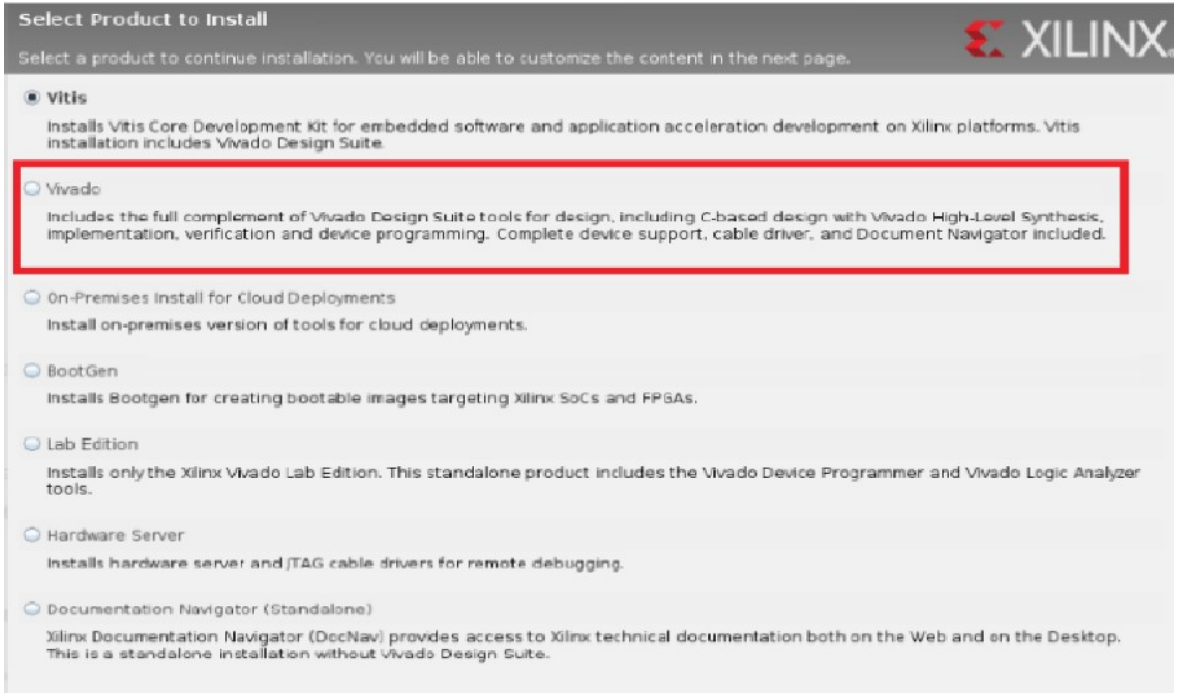
Xilinx Unified Installer 2020.2: Windows Self Extracting Web Installer (EXE - 248.44 MB)

MD5 SUM Value : 102bb67c6806a6667dc7176be7997475

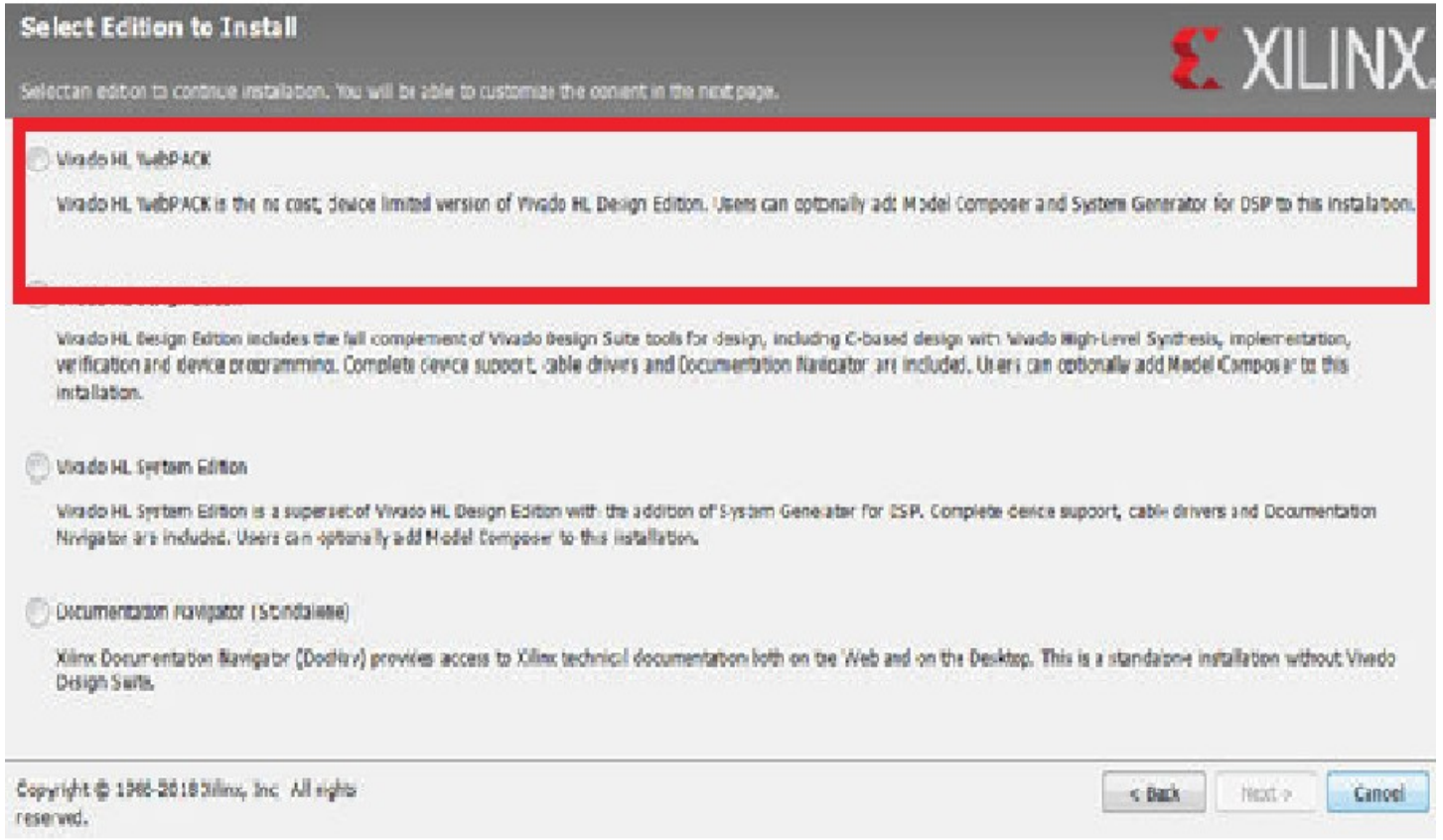
Download Verification

Digests | Signature | Public Key

Bira se Vivado



Bira se Vivado HL WebPACK



U podrazumevanoj instalaciji Vivado IDE-a nema podrške za PINQ ploče.
Link za preuzimanje datoteka za PINQ ploču:
https://vvv.tul.com.tv/productspink-z2.html

Power

- Powered from USB or 7V-15V external power source

Downloads

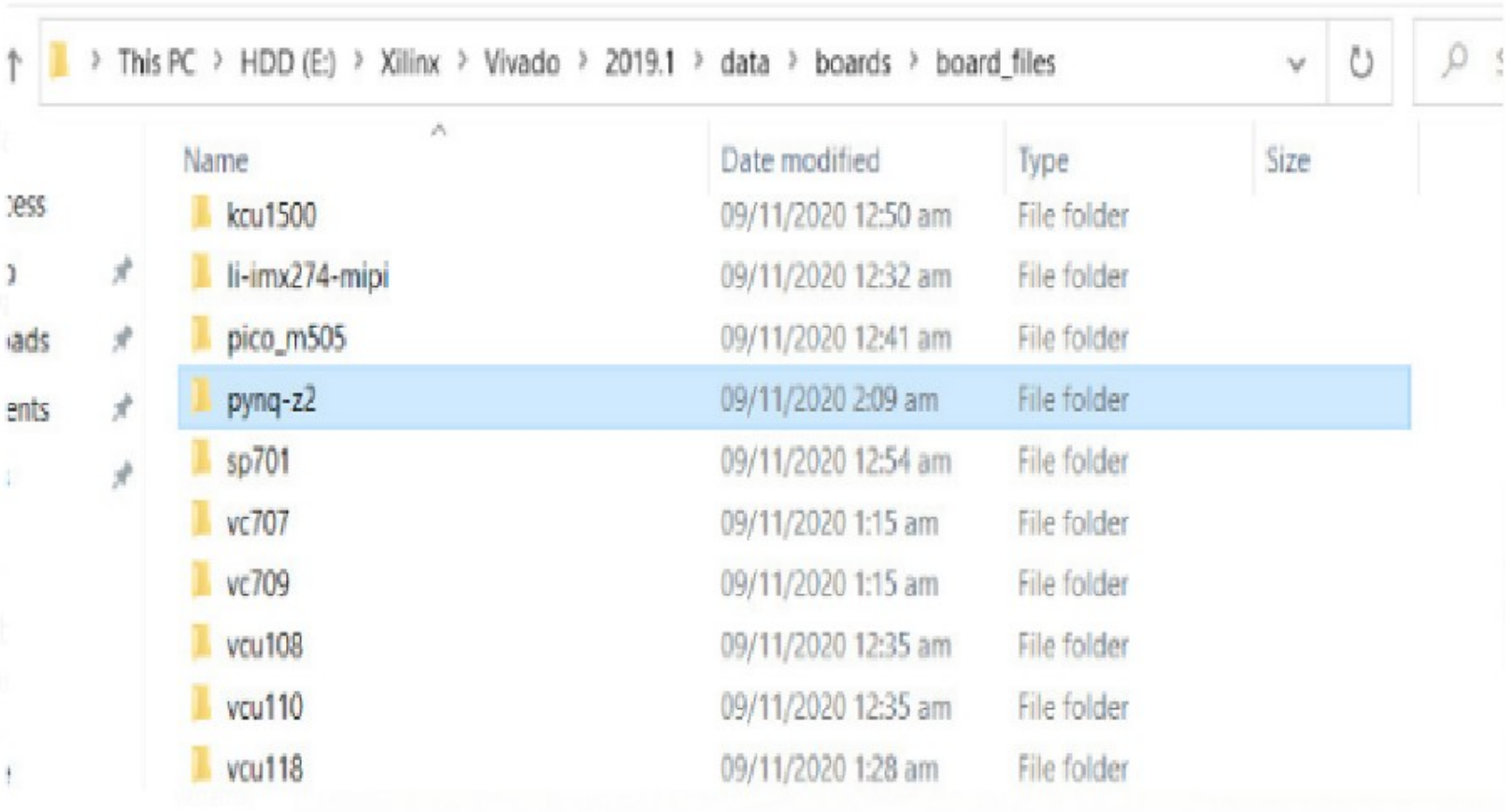
- PYNQ-Z2 User Manual (PDF)
- PYNQ-Z2 Boot Image
  1. V2.3
  2. V2.4
  3. V2.5
- PYNQ-Z2 Board File (for Pmod IP support please refere here)
- Master XDC

- Protective Acrylic Case (PDF)
- Zynq Datasheet (PDF)
- Zynq Manual (PDF)
- Schematics (PDF)

OPTIONAL

PLEASE DOWNLOAD THESE

Preuzete datoteke za plocu, kopiraju se na:
<Xilinx installation directory>\Vivado\<version>\data\boards\board_files


This PC › HDD (E:) › Xilinx › Vivado › 2019.1 › data › boards › board_files
Name
Date modified
Type
Size
kcu1500 09/11/2020 12:50 am File folder
li-imx274-mipi 09/11/2020 12:32 am File folder
pico_m505 09/11/2020 12:41 am File folder
pynq-z2 09/11/2020 2:09 am File folder
sp701 09/11/2020 12:54 am File folder
vc707 09/11/2020 1:15 am File folder
vc709 09/11/2020 1:15 am File folder
vcu108 09/11/2020 12:35 am File folder
vcu110 09/11/2020 12:35 am File folder
vcu118 09/11/2020 1:28 am File folder

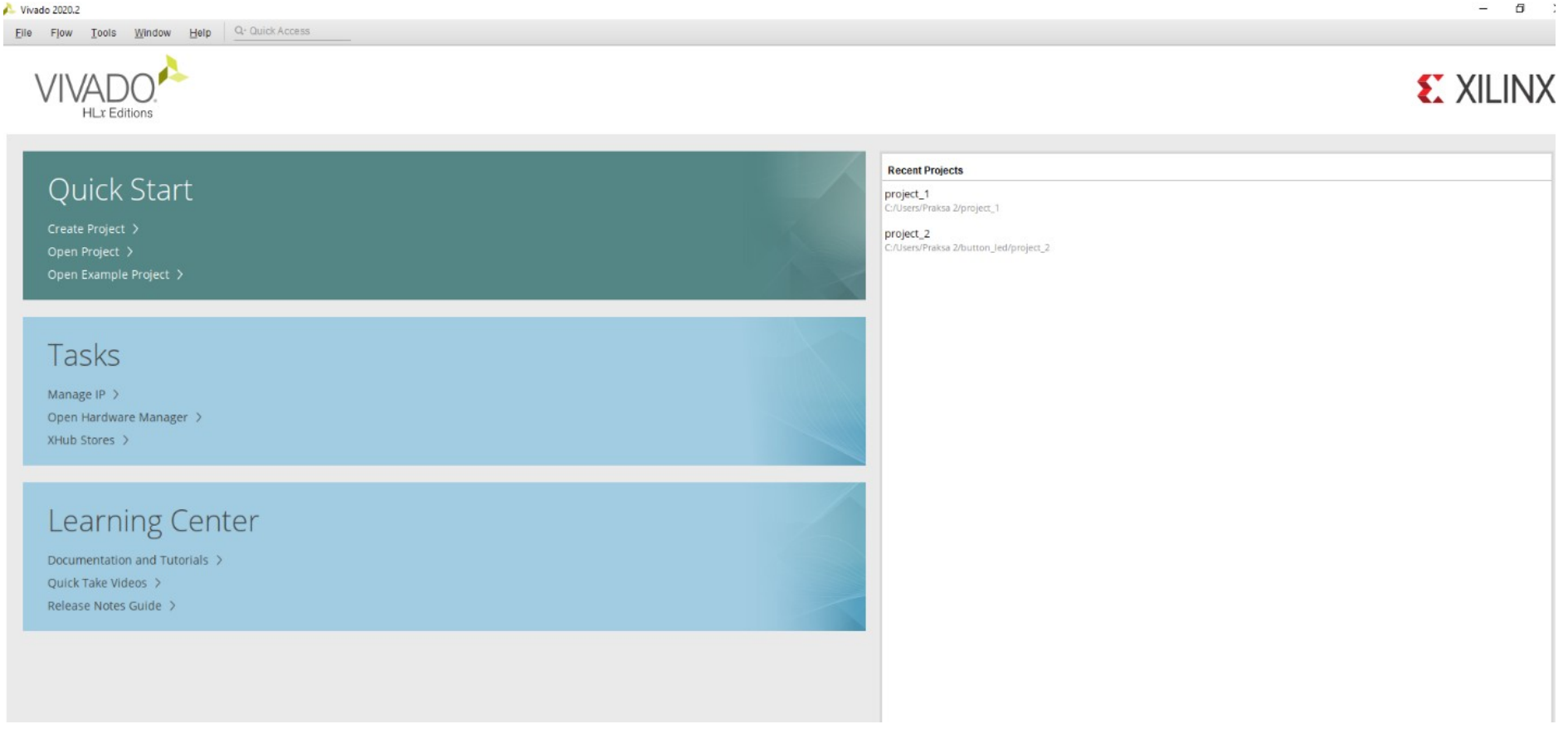
Pokretanje programa

- Windows, dupli klik na ikonu
- Linux, Ubuntu 20.04

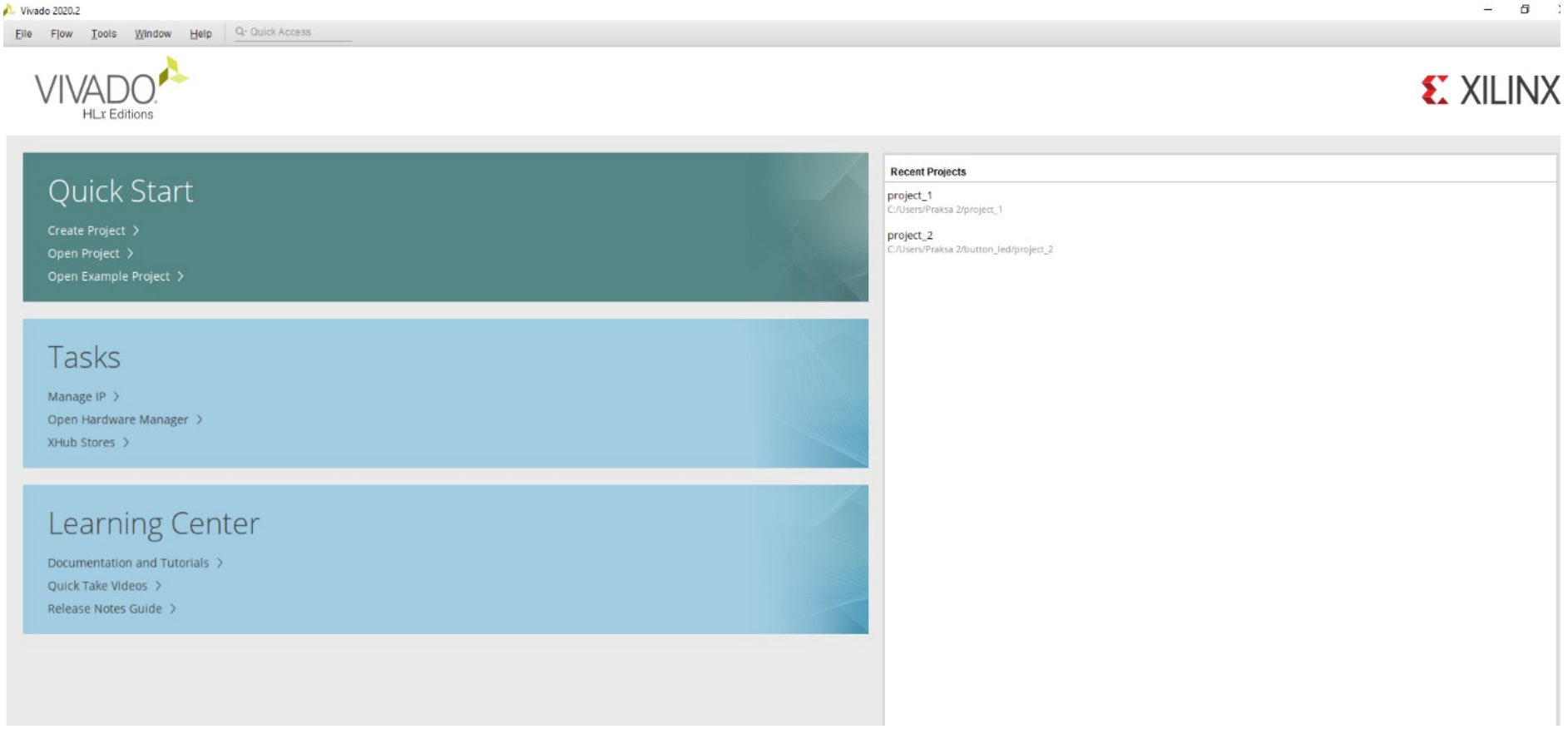
  Kao super user:

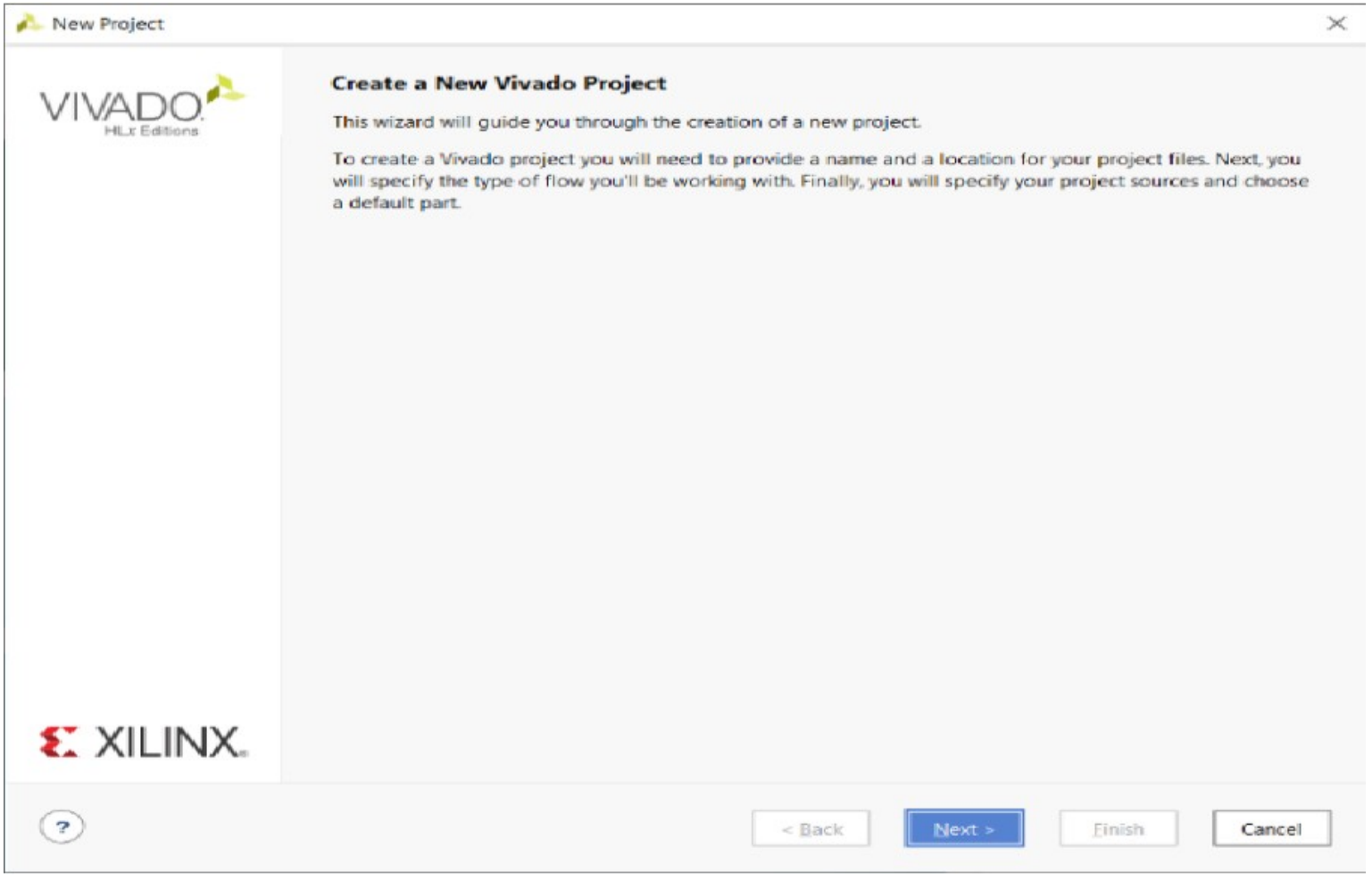
  source settings64.sh

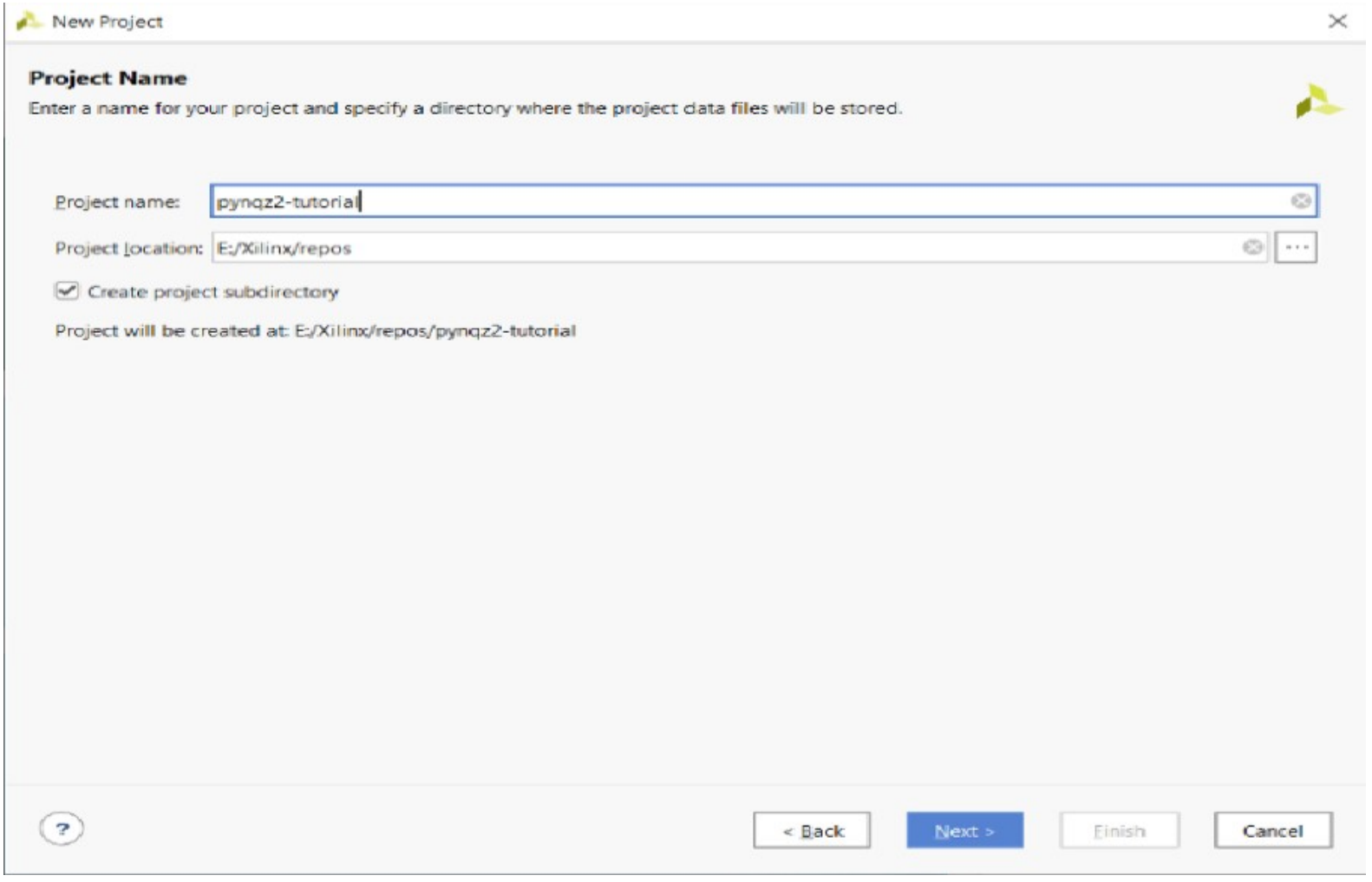
  vivado

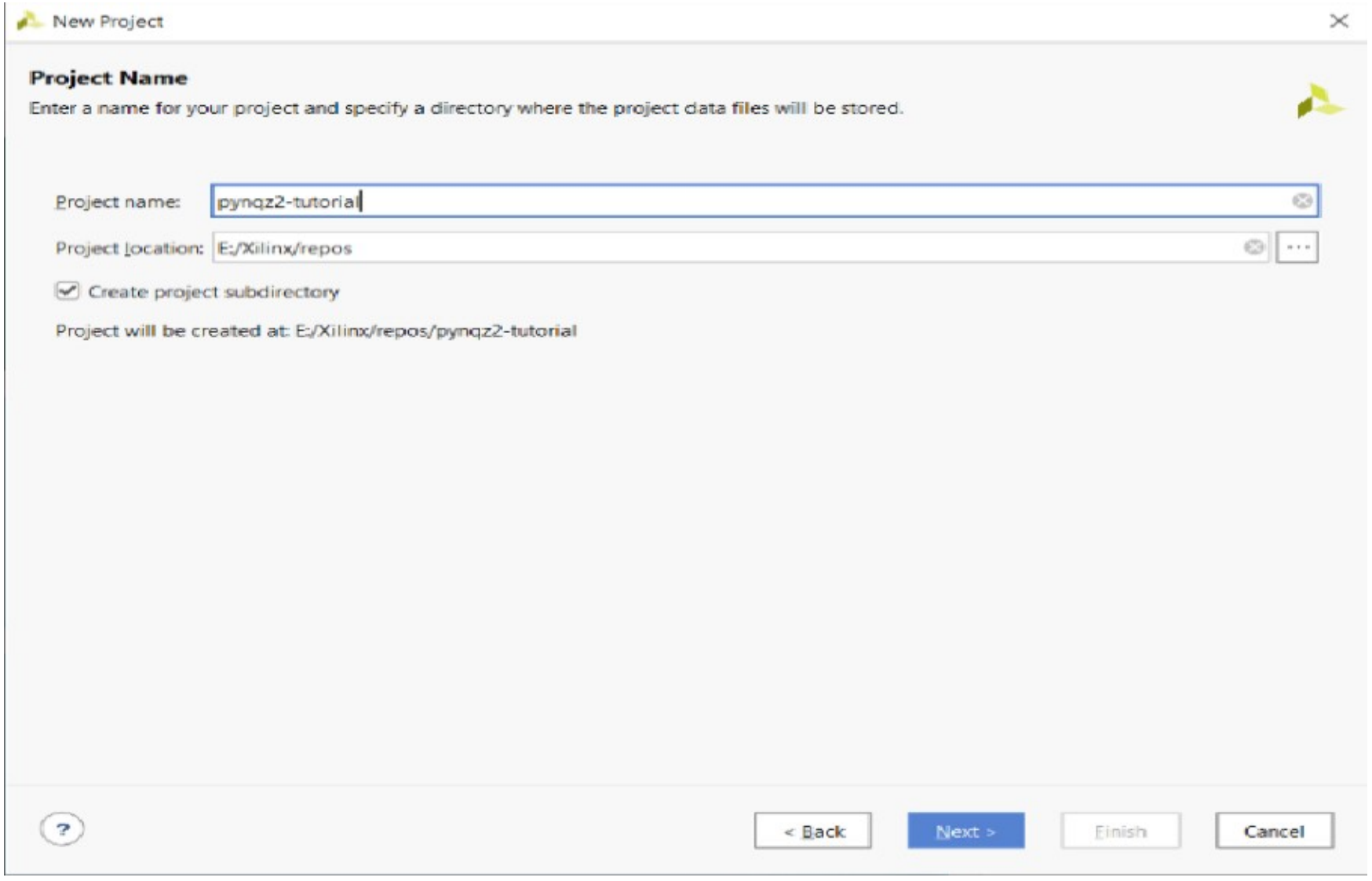

Vivado 2020.2
File
Flow
Tools
Window
Help
Quick Access
VIVADO
HLx Editions
XILINX
Quick Start
Create Project
Open Project
Open Example Project
Tasks
Manage IP
Open Hardware Manager
XHub Stores
Learning Center
Documentation and Tutorials
Quick Take Videos
Release Notes Guide
Recent Projects
project_1
C:/Users/Praksa 2/project_1
project_2
C:/Users/Praksa 2/button_led/project_2

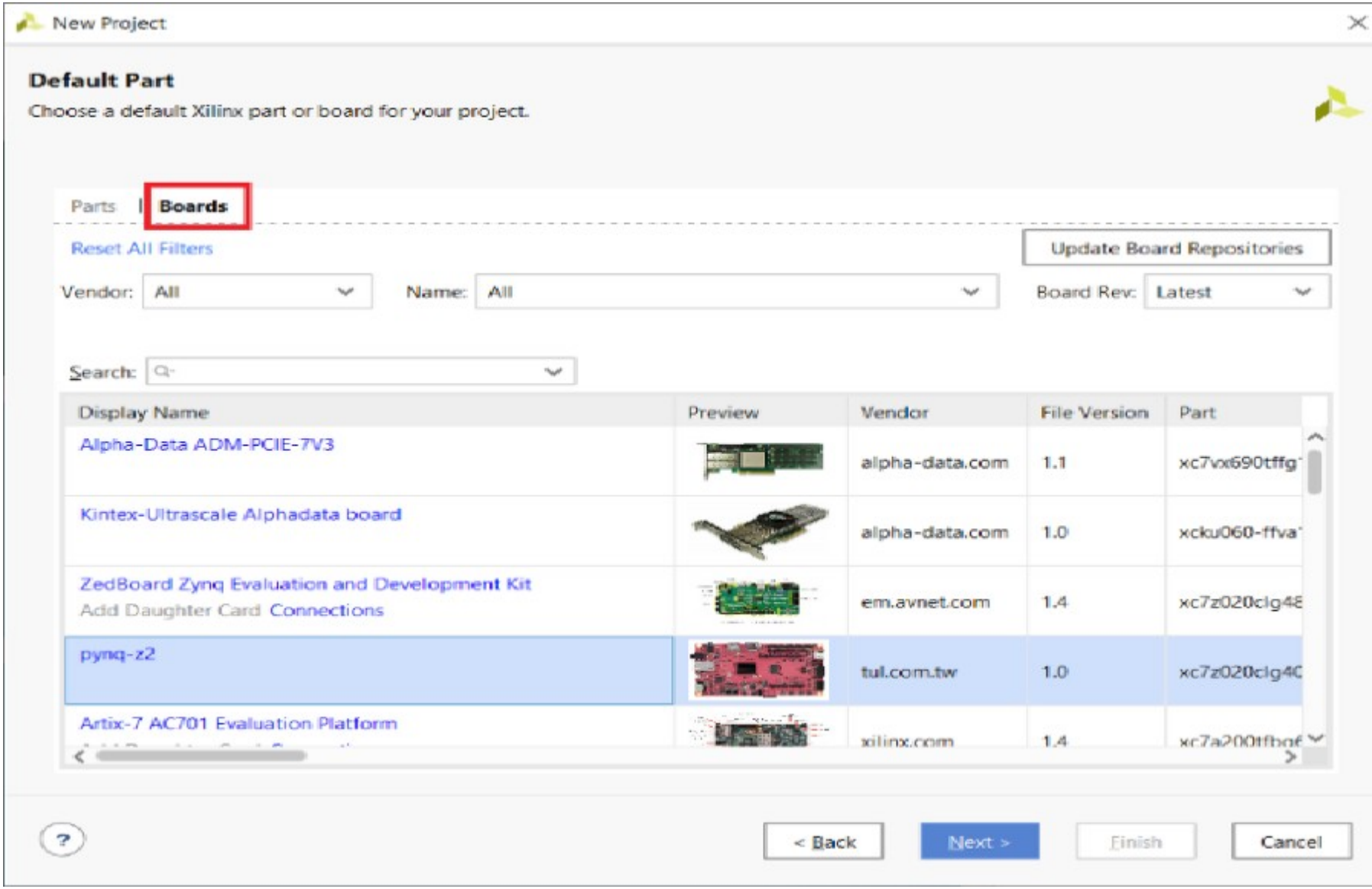
Create Project




New Project
VIVADO
HLx Editions
Create a New Vivado Project
This wizard will guide you through the creation of a new project.
To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a default part.
XILINX
?
< Back
Next >
Finish
Cancel


New Project
Project Name
Enter a name for your project and specify a directory where the project data files will be stored.
Project name:
pynqz2-tutorial
Project location:
E:/Xilinx/repos
Create project subdirectory
Project will be created at: E:/Xilinx/repos/pynqz2-tutorial
?
< Back
Next >
Finish
Cancel


New Project
Project Name
Enter a name for your project and specify a directory where the project data files will be stored.
Project name:
pynqz2-tutorial
Project location:
E:/Xilinx/repos
Create project subdirectory
Project will be created at: E:/Xilinx/repos/pynqz2-tutorial
?
< Back
Next >
Finish
Cancel


New Project
Default Part
Choose a default Xilinx part or board for your project.
Parts
Boards
Reset All Filters
Update Board Repositories
Vendor: All
Name: All
Board Rev: Latest
Search:
Display Name
Preview
Vendor
File Version
Part
Alpha-Data ADM-PCIE-7V3
alpha-data.com
1.1
Kintex-Ultrascale Alphadata board
alpha-data.com
1.0
ZedBoard Zynq Evaluation and Development Kit
Add Daughter Card Connections
em.avnet.com
1.4
pynq-z2
tul.com.tw
1.0
Artix-7 AC701 Evaluation Platform
xilinx.com
1.4
?
< Back
Next >
Finish
Cancel

project_1 - [C:/Users/Praksa 2/project_1/project_1.xpr] - Vivado 2020.2

File Edit Flow Tools Reports Window Layout View Help Quick Access

Synthesis and Implementation Out-of-date details

Default Layout

Flow Navigator

- PROJECT MANAGER
  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
  - Run Simulation
- RTL ANALYSIS
  - Open Elaborated Design
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager

PROJECT MANAGER - project_1

Sources

- Design Sources (1)
  - top (top.v)
- Constraints (1)
- Simulation Sources (1)
- Utility Sources

Hierarchy Libraries Compile Order

Properties

Select an object to see properties

Project Summary

Overview | Dashboard

Settings Edit

Project name:	project_1
Project location:	C:/Users/Praksa 2/project_1
Product family:	Zynq-7000
Project part:	pynq-z2 (xc7z020clg400-1)
Top module name:	top
Target language:	Verilog
Simulator language:	Mixed

Board Part

Display name:	pynq-z2
Board part name:	tul.com.tw:pynq-z2:part0:1.0
Board revision:	1.0
Connectors:	No connections
Repository path:	D:/Xilinx/Vivado/2020.2/data/boards/board_files
URL:	http://www.tul.com.tw
Board overview:	pynq-z2

Synthesis

Status:	Complete
Messages:	No errors or warnings
Part:	xc7z020clg400-1

Implementation Summary | Route Status

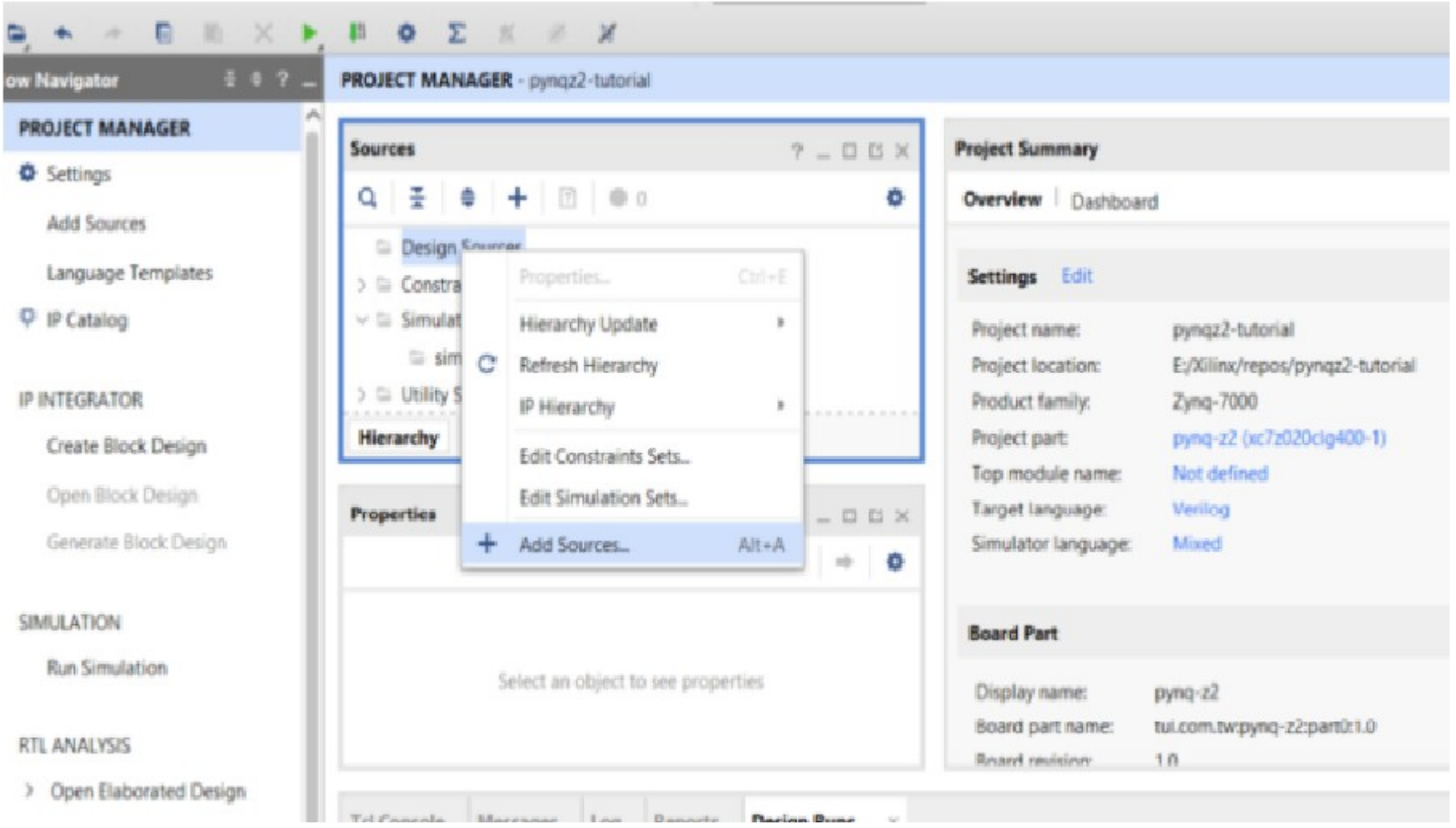
Status:	Complete
Messages:	3 warnings
Part:	xc7z020clg400-1

Tcl Console | Messages | Log | Reports | Design Runs

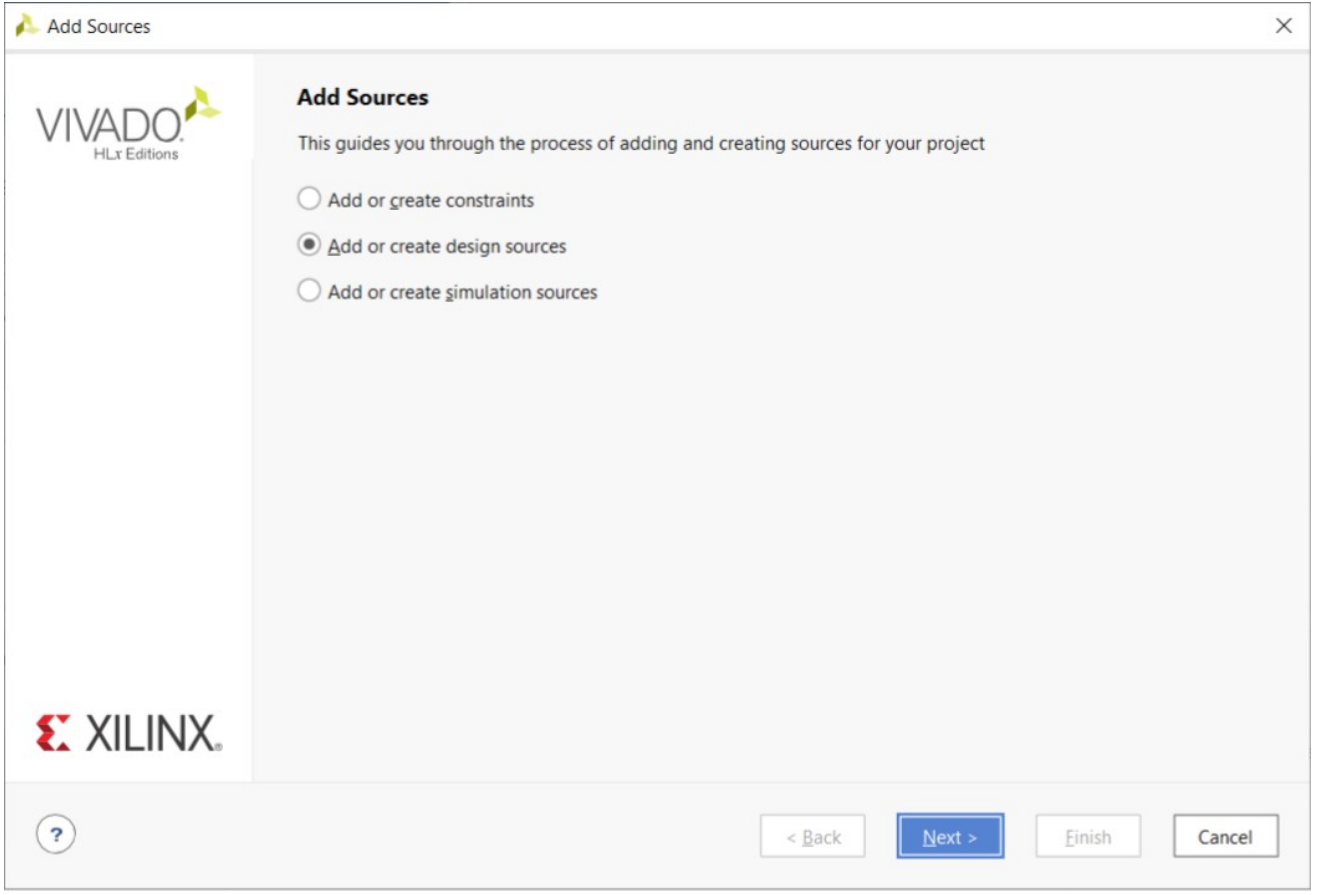
Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy

Kreiranje modula

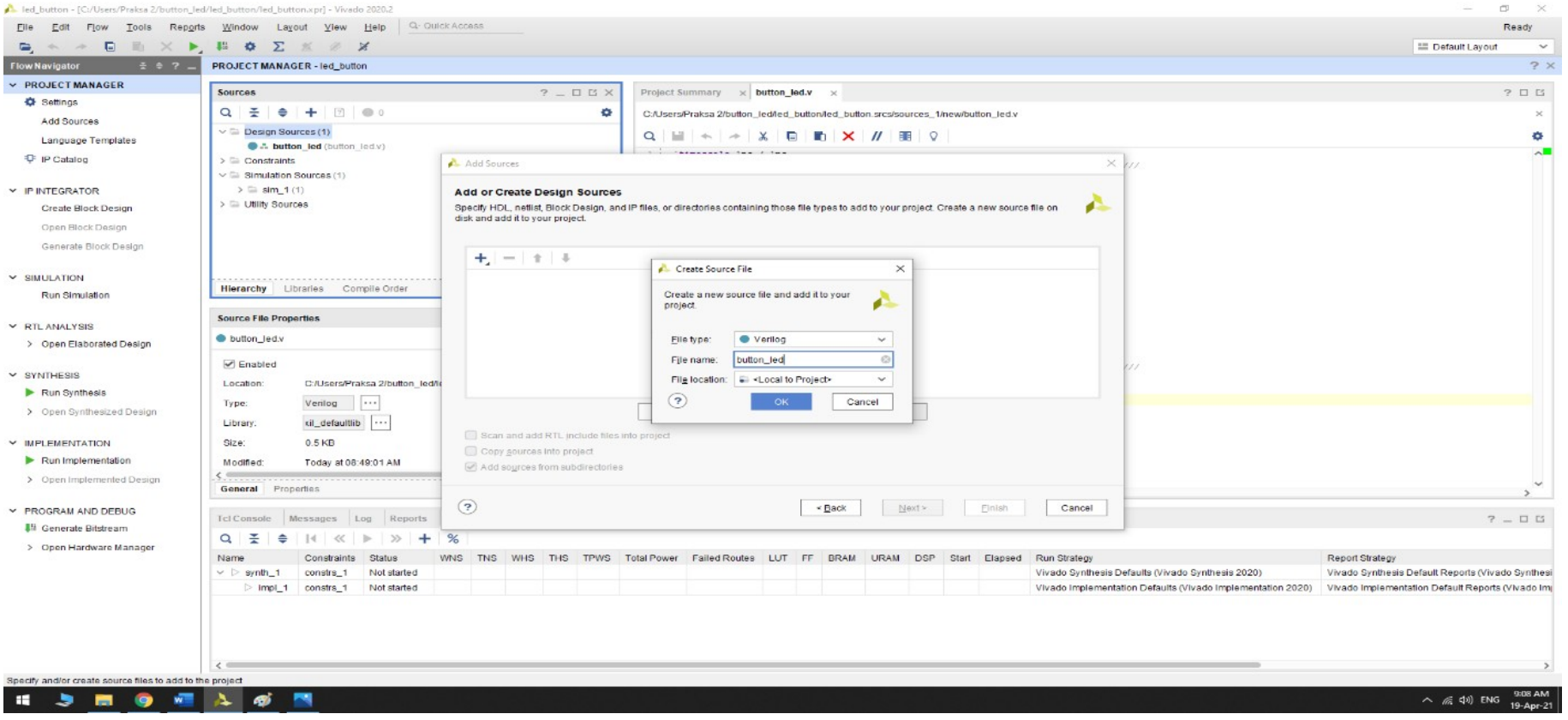
Na „Sources“ kliknite desnim tasterom miša
na „Design Sources“,
zatim kliknite na „Add sources“.


PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
PROJECT MANAGER - pynqz2-tutorial
Sources
Hierarchy
Properties
Select an object to see properties
Properties... Ctrl+E
Hierarchy Update
Refresh Hierarchy
IP Hierarchy
Edit Constraints Sets...
Edit Simulation Sets...
Add Sources... Alt+A
Project Summary
Overview
Dashboard
Settings
Edit
Project name: pynqz2-tutorial
Project location: E:/Xilinx/repos/pynqz2-tutorial
Product family: Zynq-7000
Project part: pynq-z2 (xc7z020clg400-1)
Top module name: Not defined
Target language: Verilog
Simulator language: Mixed
Board Part
Display name: pynq-z2
Board part name: tul.com.tw:pynq-z2:part0:1.0

Biramo „Add or create design sources“ i klik „Next“



„Create File“


led_button - [C:/Users/Praksa 2/button_led/led_button/led_button.xpr] - Vivado 2020.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
PROJECT MANAGER - led_button
Sources
Design Sources (1)
button_led (button_led.v)
Constraints
Simulation Sources (1)
sim_1 (1)
Utility Sources
Hierarchy Libraries Compile Order
Source File Properties
button_led.v
Enabled
Location: C:/Users/Praksa 2/button_led/l
Type: Verilog
Library: xil_defaultlib
Size: 0.5 KB
Modified: Today at 08:49:01 AM
General Properties
Project Summary
button_led.v
C:/Users/Praksa 2/button_led/led_button/led_button.srcs/sources_1/new/button_led.v
Add Sources
Add or Create Design Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.
Create Source File
Create a new source file and add it to your project.
File type: Verilog
File name: button_led
File location: <Local to Project>
OK
Cancel
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
< Back
Next >
Finish
Cancel
Tcl Console Messages Log Reports
Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAM URAM DSP Start Elapsed Run Strategy Report Strategy
synth_1 constrs_1 Not started
Vivado Synthesis Defaults (Vivado Synthesis 2020)
impl_1 constrs_1 Not started
Vivado Implementation Defaults (Vivado Implementation 2020)
Specify and/or create source files to add to the project
ENG
9:08 AM
19-Apr-21

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready

Default Layout

Flow Navigator

PROJECT MANAGER
- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR
- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION
- Run Simulation

RTL ANALYSIS
- Open Elaborated Design

SYNTHESIS
- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION
- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG
- Generate Bitstream
- Open Hardware Manager

PROJECT MANAGER - led_button

Sources

Updating

- Design Sources (1)
- Constraints
- Simulation Sources (1)
  - sim_1 (1)
- Utility Sources

Hierarchy Libraries Compile Order

Constraint Set Properties

constrs_1

Default directory: C:/Users/Praksa 2/button_led/led_button/led_bu

File count: 0

Format: XDC

Target constraint file:

Active

General Properties

Project Summary

Overview | Dashboard

Settings Edit

Project name: led_button

Project location: C:/Users/Praksa 2/button_led/led_button

Product family: Zynq-7000

Part: xc7z020clg400-1

Implementation

Status: Not started

Messages: No errors or warnings

Part: xc7z020clg400-1

Define Module

Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.

Module Definition

Module name: button_led

I/O Port Definitions

Port Name	Direction	Bus	MSB	LSB
	input		0	0

OK Cancel

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2020)	Vivado Synthesis Default Reports (Vivado Synthesi
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2020)	Vivado Implementation Default Reports (Vivado Imp

ENG 8:47 AM 19-Apr-21

PROJECT MANAGER - led_button

Sources

- Design Sources (1)
  - button_led (button_led.v)
- Constraints (1)
  - constrs_1 (1)
    - button_led_constraints.xdc
- Simulation Sources (1)
- Utility Sources

Hierarchy | Libraries | Compile Order

Source File Properties

button_led.v

Enabled

Location:	C:/Users/Praksa 2/button_led/led_button/led_button.srcs/sources_1/n
Type:	Verilog
Library:	xil_defaultlib
Size:	0.7 KB
Modified:	Today at 11:08:43 AM

General | Properties

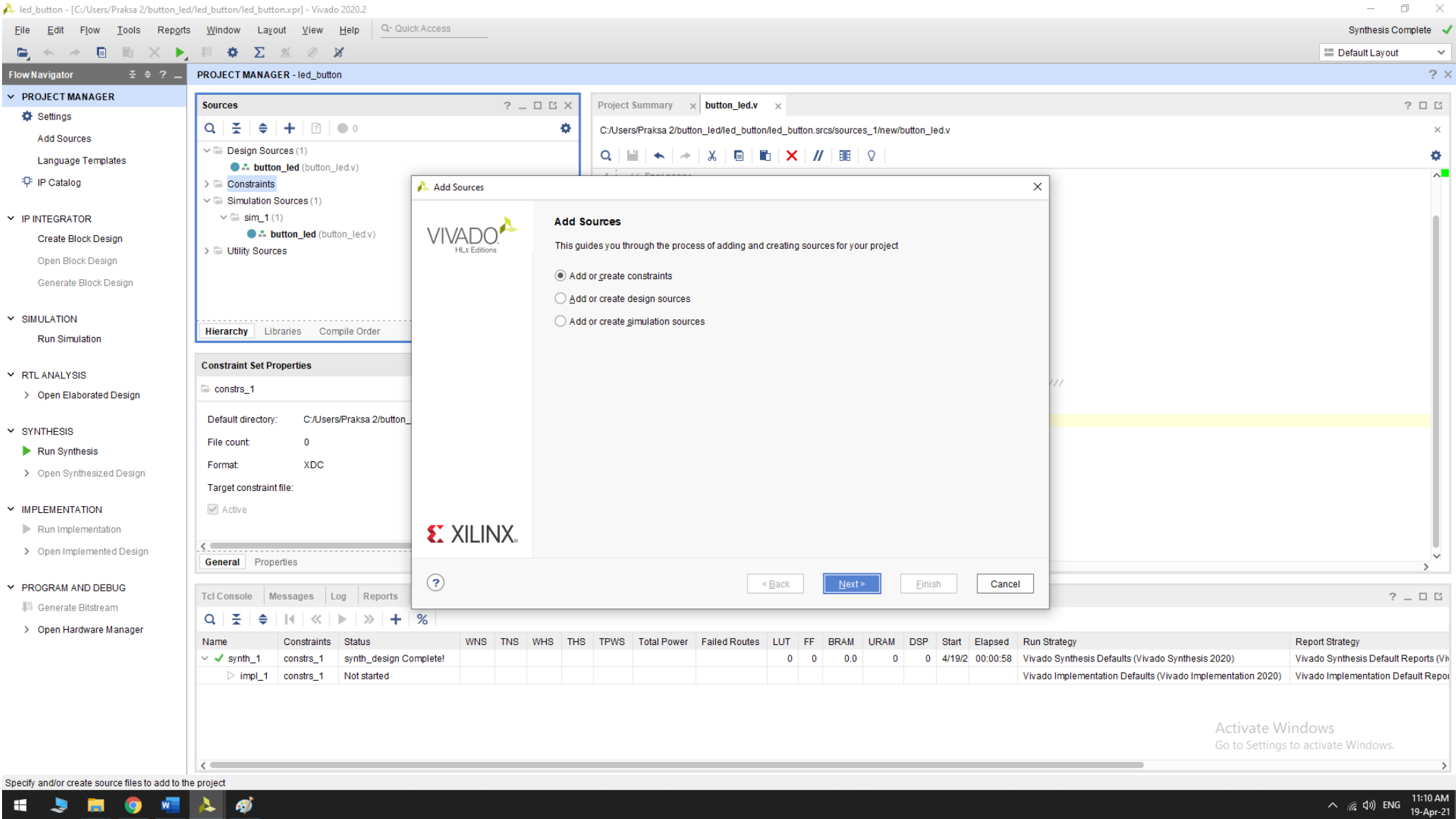
Project Summary | button_led.v | button_led_constraints.xdc

C:/Users/Praksa 2/button_led/led_button/led_button.srcs/sources_1/new/button_led.v

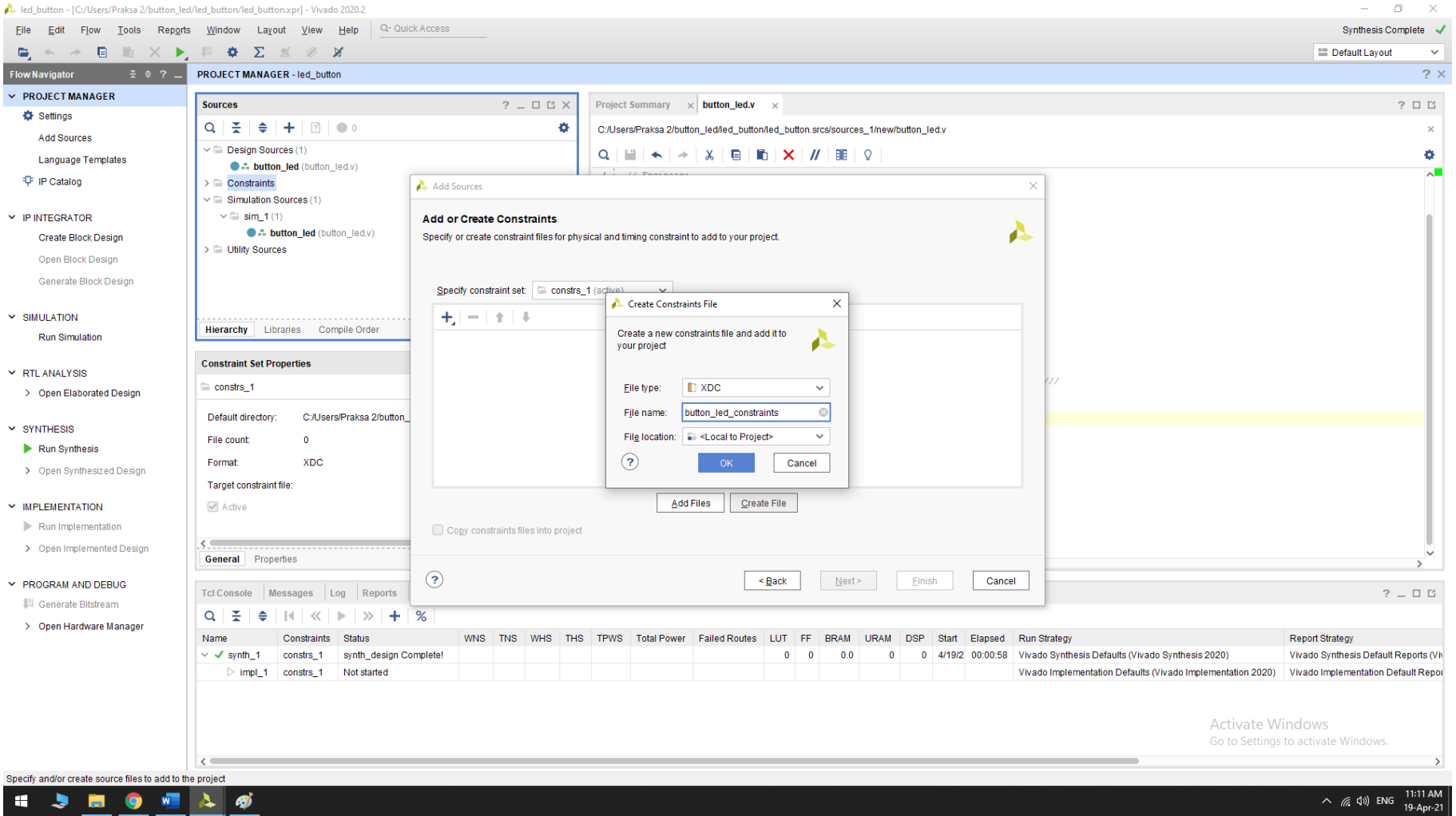
```
4  // Engineer:
5  //
6  // Create Date: 04/19/2021 08:49:01 AM
7  // Design Name:
8  // Module Name: button_led
9  // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////////////////////////////////////


23 module button_led(input button0, input button1, input button2, input button3,
24 output led0, output led1, output led2, output led3 );
25
26 assign led0 = button0;
27 assign led1 = button1;
28 assign led2 = button2;
29 assign led3 = button3;
30
31
32 endmodule
33
```

Tcl Console | Messages | Log | Reports | Design Runs

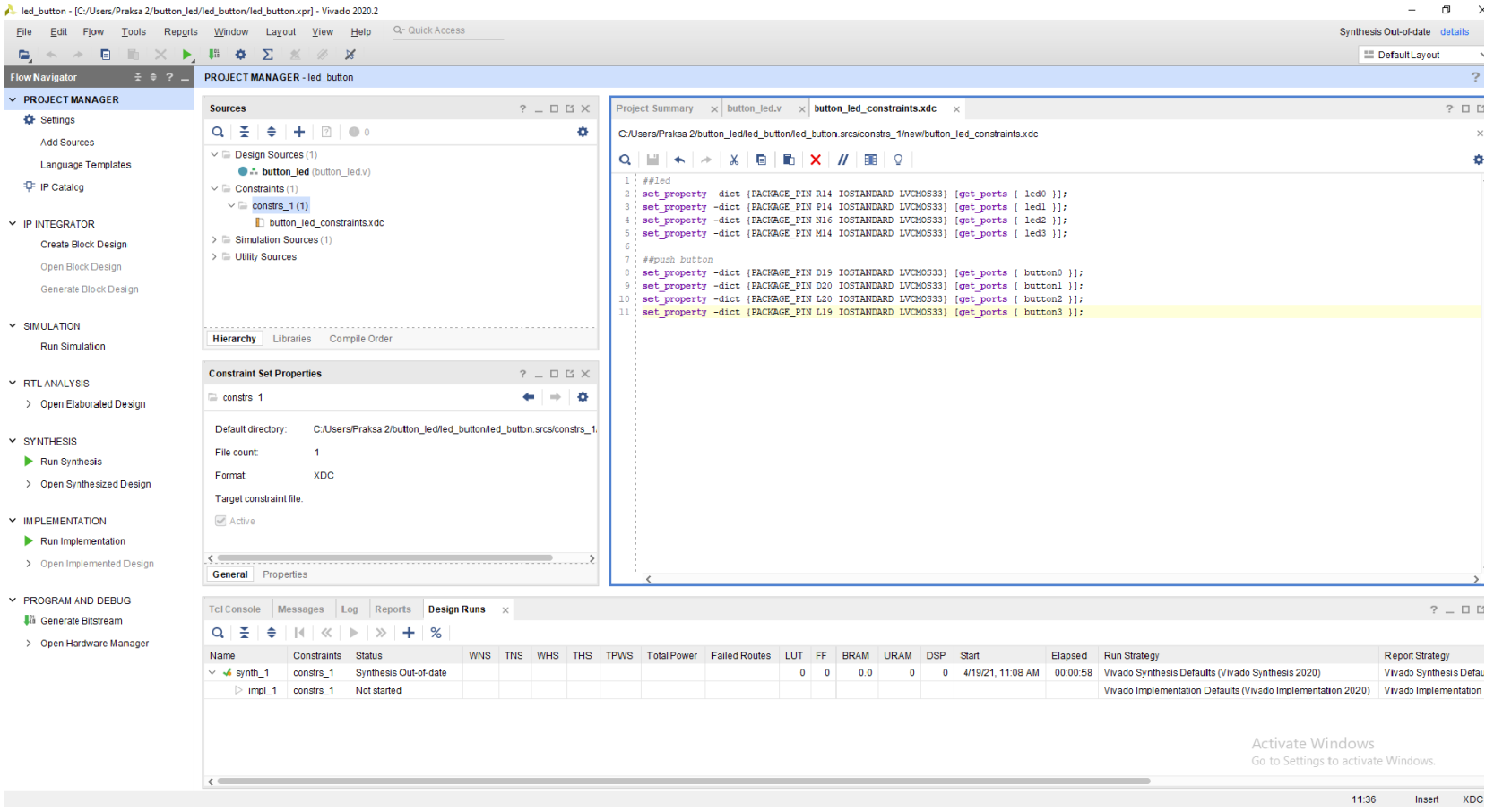
Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy


led_button - [C:/Users/Praksa 2/button_led/led_button/led_button.xpr] - Vivado 2020.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Synthesis Complete
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
PROJECT MANAGER - led_button
Sources
Design Sources (1)
button_led (button_led.v)
Constraints
Simulation Sources (1)
sim_1 (1)
button_led (button_led.v)
Utility Sources
Hierarchy Libraries Compile Order
Project Summary
button_led.v
C:/Users/Praksa 2/button_led/led_button/led_button.srcs/sources_1/new/button_led.v
Constraint Set Properties
constrs_1
Default directory: C:/Users/Praksa 2/button_
File count: 0
Format: XDC
Target constraint file:
Active
General Properties
Add Sources
VIVADO HLx Editions
Add Sources
This guides you through the process of adding and creating sources for your project
Add or create constraints
Add or create design sources
Add or create simulation sources
XILINX
< Back
Next >
Finish
Cancel
Tcl Console Messages Log Reports
Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAM URAM DSP Start Elapsed Run Strategy Report Strategy
synth_1 constrs_1 synth_design Complete! 0 0 0.0 0 0 4/19/2 00:00:58 Vivado Synthesis Defaults (Vivado Synthesis 2020) Vivado Synthesis Default Reports (Vi
impl_1 constrs_1 Not started Vivado Implementation Defaults (Vivado Implementation 2020) Vivado Implementation Default Repo
Activate Windows
Go to Settings to activate Windows.
Specify and/or create source files to add to the project
ENG
11:10 AM
19-Apr-21

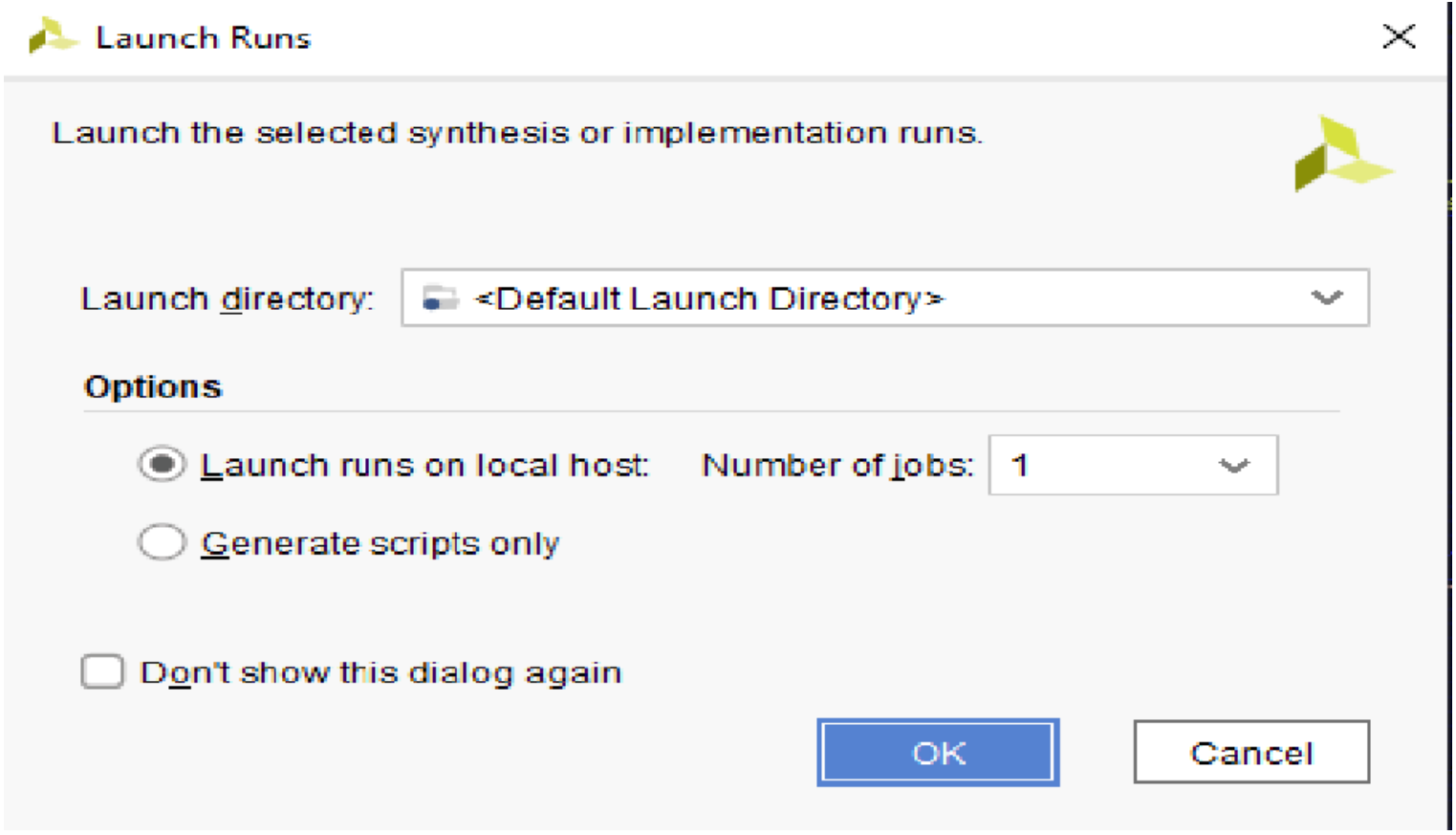
U „Add sources“ biramo „Add or create constraints“ i klinknemo „Next“



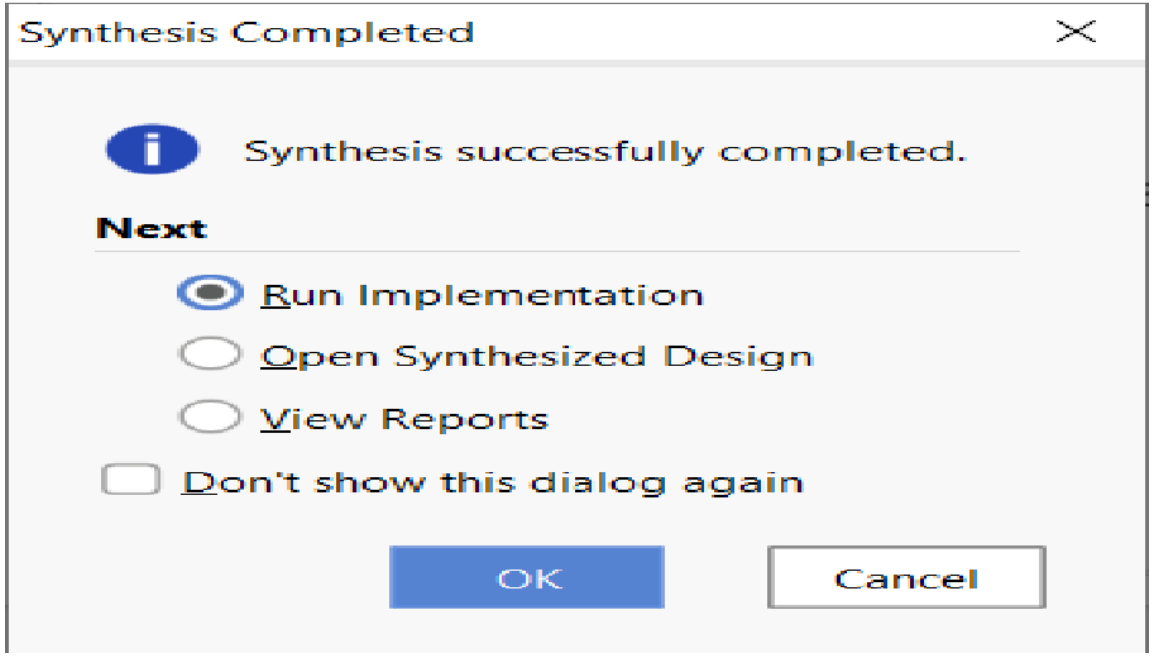
Definisemo pinove



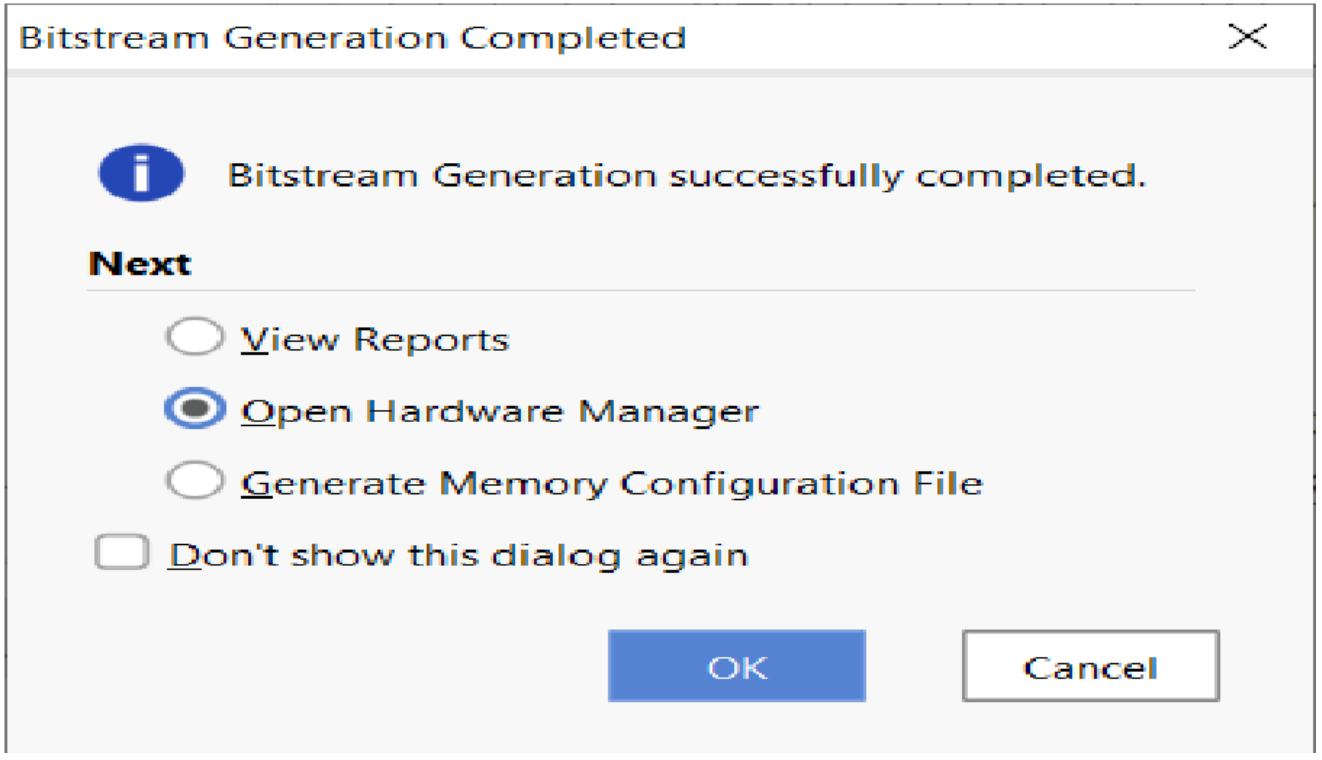
Run Synthesis



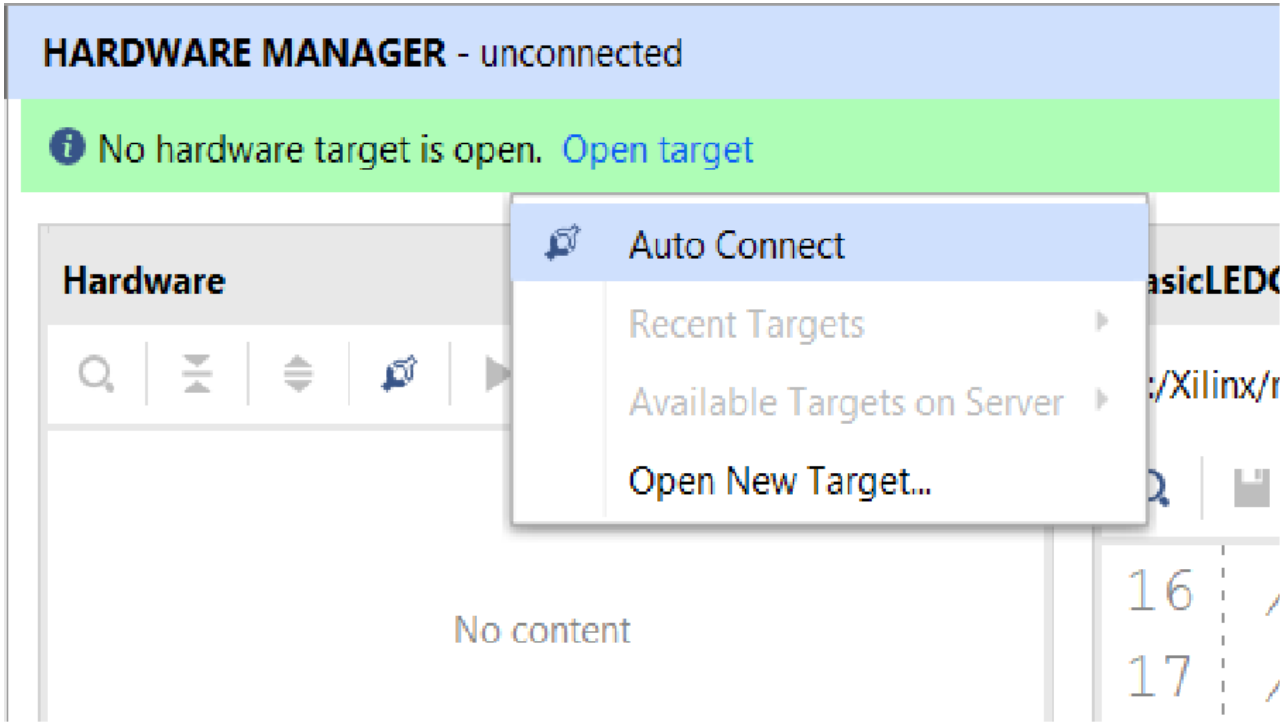
Run Implementation

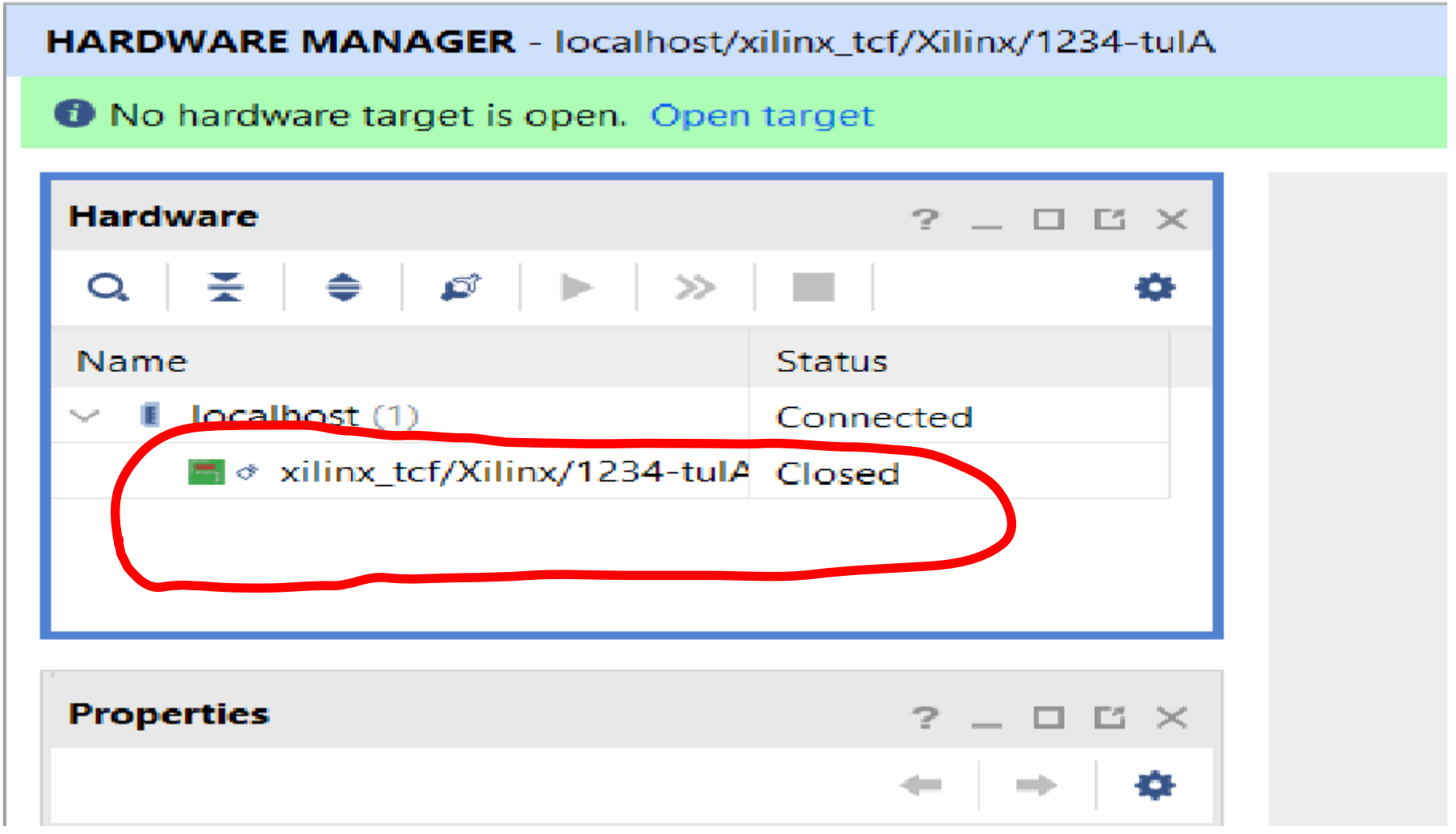


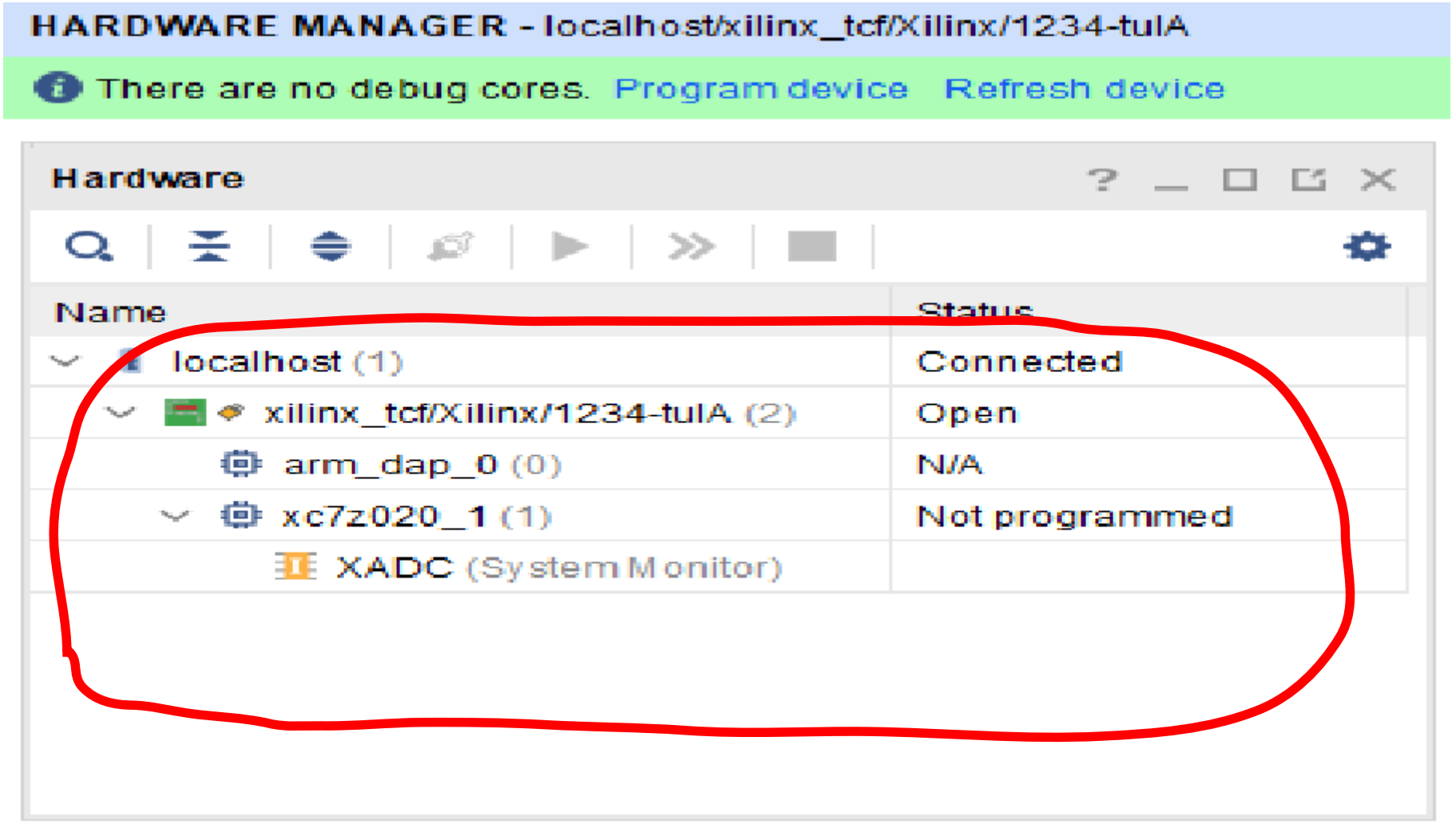
Generisanje Bitstream i programirajte FPGA

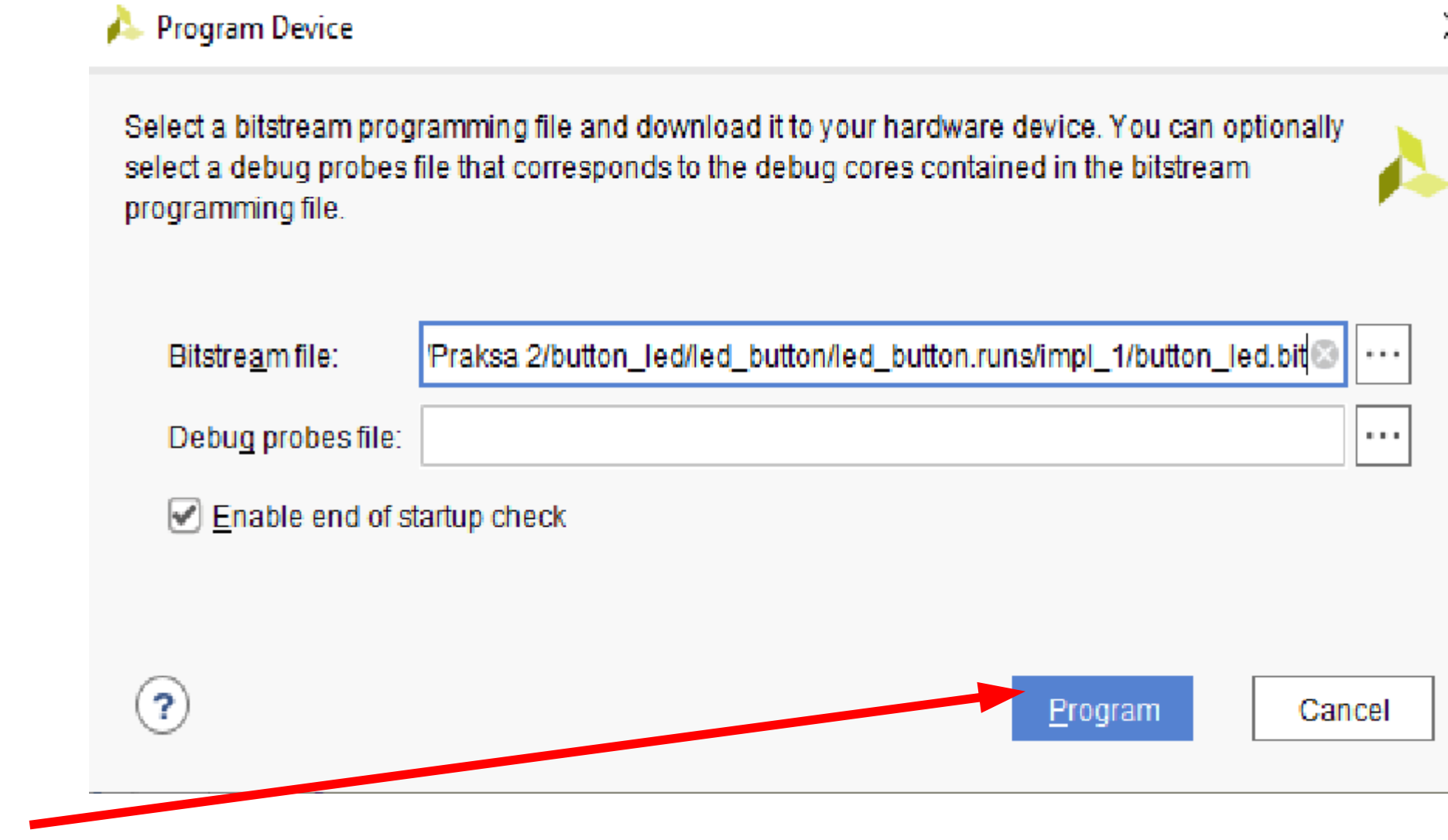


Open target, zatim Auto Connect




HARDWARE MANAGER - localhost/xilinx_tcf/Xilinx/1234-tulA
No hardware target is open. Open target
Hardware
Name
Status
localhost (1)
Connected
xilinx_tcf/Xilinx/1234-tulA
Closed
Properties


HARDWARE MANAGER - localhost/xilinx_tcf/Xilinx/1234-tulA
There are no debug cores. Program device Refresh device
Hardware
Name
Status
localhost (1)
Connected
xilinx_tcf/Xilinx/1234-tulA (2)
Open
arm_dap_0 (0)
N/A
xc7z020_1 (1)
Not programmed
XADC (System Monitor)


Program Device
Select a bitstream programming file and download it to your hardware device. You can optionally select a debug probes file that corresponds to the debug cores contained in the bitstream programming file.
Bitstream file:
Praksa 2/button_led/led_button/led_button.runs/impl_1/button_led.bit
Debug probes file:
Enable end of startup check
Program
Cancel

Program moze da se testira!
Klik na taster, ukljucuje se LED!