

# Vivado-Instalacija programa

Instalacija je dostupna za slobodno preuzimanje sa sledećeg linka:

<https://www.xilinx.com/support/download.html>

Napomena:

Vivado ne podržava 32-bitne procesore.

 [Xilinx Unified Installer 2020.2: Windows Self Extracting Web Installer \(EXE - 248.44 MB\)](#)

MD5 SUM Value : 102bb67c6806a6667dc7176be7997475


Download Verification 

Digests

Signature

Public Key

# Bira se Vivado


Select Product to Install 

Select a product to continue installation. You will be able to customize the content in the next page.

- Vitis**  
Installs Vitis Core Development Kit for embedded software and application acceleration development on Xilinx platforms. Vitis installation includes Vivado Design Suite.
- Vivado**  
Includes the full complement of Vivado Design Suite tools for design, including C-based design with Vivado High-Level Synthesis, implementation, verification and device programming. Complete device support, cable driver, and Document Navigator included.
- On-Premises Install for Cloud Deployments**  
Install on-premises version of tools for cloud deployments.
- BootGen**  
Installs Bootgen for creating bootable images targeting Xilinx SoCs and FPGAs.
- Lab Edition**  
Installs only the Xilinx Vivado Lab Edition. This standalone product includes the Vivado Device Programmer and Vivado Logic Analyzer tools.
- Hardware Server**  
Installs hardware server and JTAG cable drivers for remote debugging.
- Documentation Navigator (Standalone)**  
Xilinx Documentation Navigator (DocNav) provides access to Xilinx technical documentation both on the Web and on the Desktop. This is a standalone installation without Vivado Design Suite.

# Bira se Vivado HL WebPACK

## Select Edition to Install



Select an edition to continue installation. You will be able to customize the content in the next page.

- Vivado HL WebPACK**

Vivado HL WebPACK is the no cost, device limited version of Vivado HL Design Edition. Users can optionally add Model Composer and System Generator for DSP to this installation.
- Vivado HL System Edition**

Vivado HL System Edition is a superset of Vivado HL Design Edition with the addition of System Generator for DSP. Complete device support, cable drivers and Documentation Navigator are included. Users can optionally add Model Composer to this installation.
- Documentation Navigator (Standalone)**

Xilinx Documentation Navigator (DocNav) provides access to Xilinx technical documentation both on the Web and on the Desktop. This is a standalone installation without Vivado Design Suite.

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U podrazumevanoj instalaciji Vivado IDE-a nema podrške za PINQ ploče.

Link za preuzimanje datoteka za PINQ ploču:

<https://vvv.tul.com.tv/productspink-z2.html>

Power

- Powered from USB or 7V-15V external power source

Downloads

- PYNQ-Z2 User Manual (PDF)

- PYNQ-Z2 Boot Image

1. V2.3

2. V2.4

3. V2.5

- PYNQ-Z2 Board File (for Pmod IP support please refer here)

- Master XDC

- Protective Acrylic Case (PDF)

- Zynq Datasheet (PDF)

- Zynq Manual (PDF)

- Schematics (PDF)

**OPTIONAL**

**PLEASE  
DOWNLOAD  
THESE**

Order

Technical Support

Preuzete datoteke za ploču, kopiraju se na:

<Xilinx installation directory>\Vivado\<version>\data\  
boards\board\_files

↑ > This PC > HDD (E:) > Xilinx > Vivado > 2019.1 > data > boards > board\_files

	Name	Date modified	Type	Size
ess	ku1500	09/11/2020 12:50 am	File folder	
o	li-imx274-mipi	09/11/2020 12:32 am	File folder	
ads	pico_m505	09/11/2020 12:41 am	File folder	
ents	pynq-z2	09/11/2020 2:09 am	File folder	
	sp701	09/11/2020 12:54 am	File folder	
	vc707	09/11/2020 1:15 am	File folder	
	vc709	09/11/2020 1:15 am	File folder	
	vcu108	09/11/2020 12:35 am	File folder	
	vcu110	09/11/2020 12:35 am	File folder	
	vcu118	09/11/2020 1:28 am	File folder	



# Pokretanje programa

- Windows, dupli klik na ikonu
- Linux, Ubuntu 20.04

Kao super user:

```
source settings64.sh
```

```
vivado
```



## Quick Start

- [Create Project >](#)
- [Open Project >](#)
- [Open Example Project >](#)

## Tasks

- [Manage IP >](#)
- [Open Hardware Manager >](#)
- [XHub Stores >](#)

## Learning Center

- [Documentation and Tutorials >](#)
- [Quick Take Videos >](#)
- [Release Notes Guide >](#)

### Recent Projects

- project\_1**  
C:/Users/Praksa 2/project\_1
- project\_2**  
C:/Users/Praksa 2/button\_led/project\_2

# Create Project

Vivado 2020.2

File Flow Tools Window Help Q: Quick Access

VIVADO  
HLx Editions

XILINX

## Quick Start

- [Create Project >](#)
- [Open Project >](#)
- [Open Example Project >](#)

## Tasks

- [Manage IP >](#)
- [Open Hardware Manager >](#)
- [XHub Stores >](#)

## Learning Center

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### Recent Projects

- project\_1**  
C:/Users/Praksa 2/project\_1
- project\_2**  
C:/Users/Praksa 2/button\_led/project\_2



### Create a New Vivado Project

This wizard will guide you through the creation of a new project.

To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a default part.



&lt; Back

Next &gt;

Finish

Cancel

**Project Name**

Enter a name for your project and specify a directory where the project data files will be stored.



Project name:

Project location:

Create project subdirectory

Project will be created at: E:/Xilinx/repos/pynqz2-tutorial



< Back

Next >

Finish

Cancel

## Project Name

Enter a name for your project and specify a directory where the project data files will be stored.



Project name:

Project location:

Create project subdirectory

Project will be created at: E:/Xilinx/repos/pynqz2-tutorial



## Default Part

Choose a default Xilinx part or board for your project.



Parts






**Boards**[Reset All Filters](#)[Update Board Repositories](#)

Vendor: All

Name: All

Board Rev: Latest

Search: 

Display Name	Preview	Vendor	File Version	Part
<a href="#">Alpha-Data ADM-PCIE-7V3</a>		alpha-data.com	1.1	xc7vx690tffg
<a href="#">Kintex-Ultrascale Alphadata board</a>		alpha-data.com	1.0	xcku060-ffva
<a href="#">ZedBoard Zynq Evaluation and Development Kit</a> <a href="#">Add Daughter Card Connections</a>		em.avnet.com	1.4	xc7z020clg4E
<a href="#">pynq-z2</a>		tul.com.tw	1.0	xc7z020clg4C
<a href="#">Artix-7 AC701 Evaluation Platform</a>		xilinx.com	1.4	xc7a2001fbbqf



&lt; Back

Next &gt;

Finish

Cancel





# Kreiranje modula

Na „Sources“ kliknite desnim tasterom miša  
na „Design Sources“,  
zatim kliknite na „Add sources“.

**Project Manager - pynqz2-tutorial**

**Sources**

- Design
- Constra
- Simulat
- sim
- Utility S
- Hierarchy**

**Context Menu:**

- Properties... (Ctrl+E)
- Hierarchy Update
- Refresh Hierarchy
- IP Hierarchy
- Edit Constraints Sets...
- Edit Simulation Sets...
- + Add Sources... (Alt+A)**

**Project Summary**

**Overview** | Dashboard

**Settings** | Edit

Project name:	pynqz2-tutorial
Project location:	E:/Xilinx/repos/pynqz2-tutorial
Product family:	Zynq-7000
Project part:	pynq-z2 (xc7z020clg400-1)
Top module name:	Not defined
Target language:	Verilog
Simulator language:	Mixed

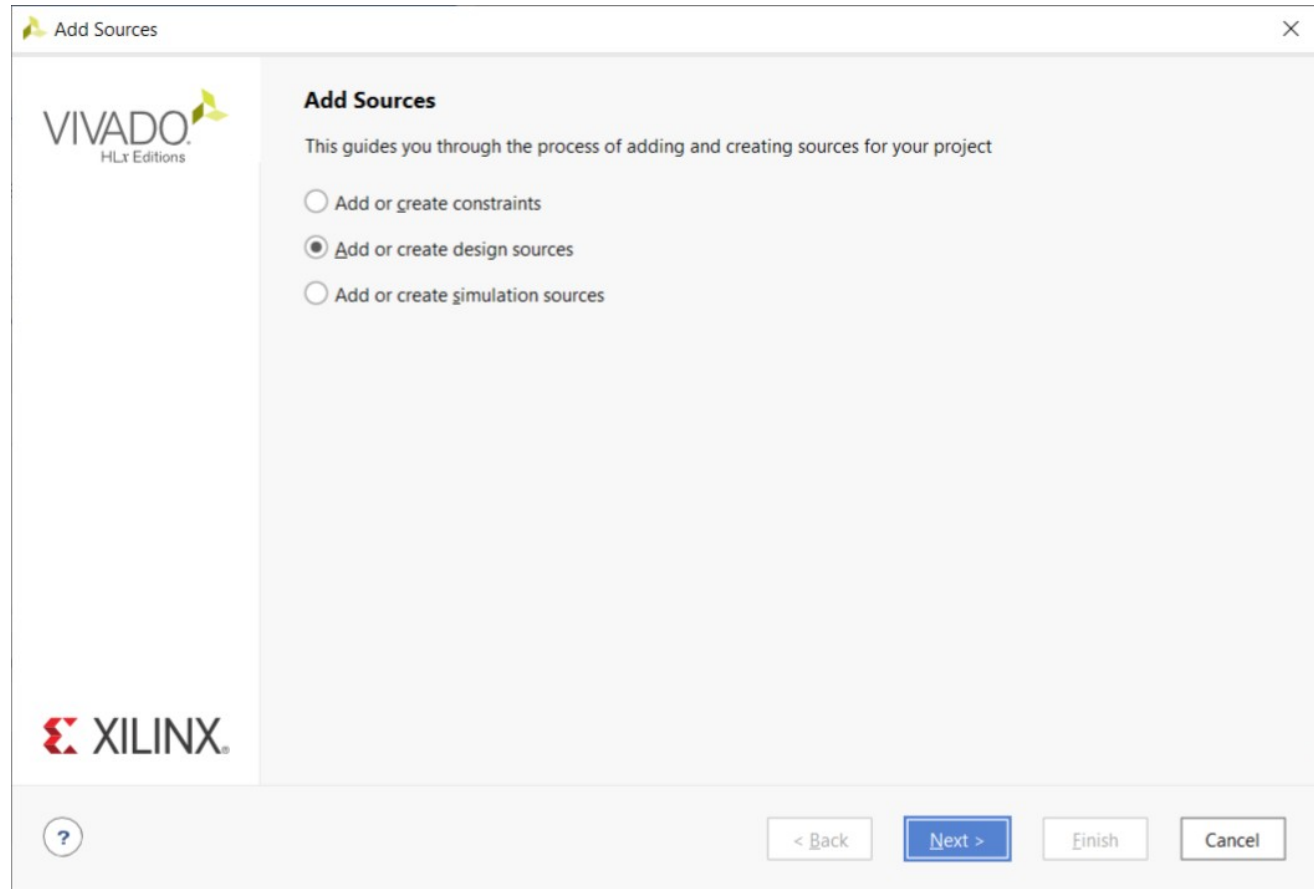
**Board Part**

Display name:	pynq-z2
Board part name:	tul.com.tw:pynq-z2:part0:1.0
Board revision:	1.0

**Properties**

Select an object to see properties

Biramo „Add or create design sources“  
i klik „Next“



# „Create File“

The screenshot displays the Vivado 2020.2 software interface. The main window is titled "led\_button - [C:/Users/Praksa 2/button\_led/led\_button/led\_button.prj] - Vivado 2020.2". The "PROJECT MANAGER" panel on the left shows a tree view with "button\_led (button\_led.v)" selected under "Design Sources (1)". The "Source File Properties" panel shows details for "button\_led.v", including its location, type (Verilog), library (xil\_defaultlib), and size (0.5 KB). The "Add or Create Design Sources" dialog box is open, with the "Create Source File" sub-dialog box also open. The "Create Source File" dialog shows "File type: Verilog", "File name: button\_led", and "File location: <Local to Project>". The "General" tab of the dialog is active, and the "OK" button is highlighted. The background shows the "Project Summary" and "button\_led.v" tabs, and the "Hierarchy" view of the design.

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2020)	Vivado Synthesis Default Reports (Vivado Synthesis 2020)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2020)	Vivado Implementation Default Reports (Vivado Implementation 2020)

Specify and/or create source files to add to the project

9:08 AM 19-Apr-21

**PROJECT MANAGER**

- Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
  - Run Simulation
- RTL ANALYSIS
  - Open Elaborated Design
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager

**Sources** Updating

- Design Sources (1)
- Constraints
- Simulation Sources (1)
  - sim\_1 (1)
- Utility Sources

Hierarchy Libraries Compile Order

**Constraint Set Properties**

constrs\_1

Default directory: C:/Users/Praksa 2/button\_led/led\_button/led\_button

File count: 0

Format: XDC

Target constraint file:

Active

General Properties

**Project Summary** Overview | Dashboard

Settings Edit

Project name: led\_button  
 Project location: C:/Users/Praksa 2/button\_led/led\_button  
 Product family: Zynq-7000

**Define Module**

Define a module and specify I/O Ports to add to your source file.  
 For each port specified:  
 MSB and LSB values will be ignored unless its Bus column is checked.  
 Ports with blank names will not be written.

**Module Definition**

Module name: button\_led

**I/O Port Definitions**

Port Name	Direction	Bus	MSB	LSB
	input	<input type="checkbox"/>	0	0

OK Cancel

Part: xc7z020clg400-1

**Implementation**

Status: Not started  
 Messages: No errors or warnings  
 Part: xc7z020clg400-1

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2020)	Vivado Synthesis Default Reports (Vivado Synthesis 2020)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2020)	Vivado Implementation Default Reports (Vivado Implementation 2020)



### Sources

Design Sources (1)  
  ● button\_led (button\_led.v)

Constraints (1)  
  constrs\_1 (1)  
    button\_led\_constraints.xdc

Simulation Sources (1)

Utility Sources

Hierarchy Libraries Compile Order

### Source File Properties

button\_led.v

Enabled

Location: C:/Users/Praksa 2/button\_led/led\_button/led\_button.srcs/sources\_1/n

Type: Verilog

Library: xil\_defaultlib

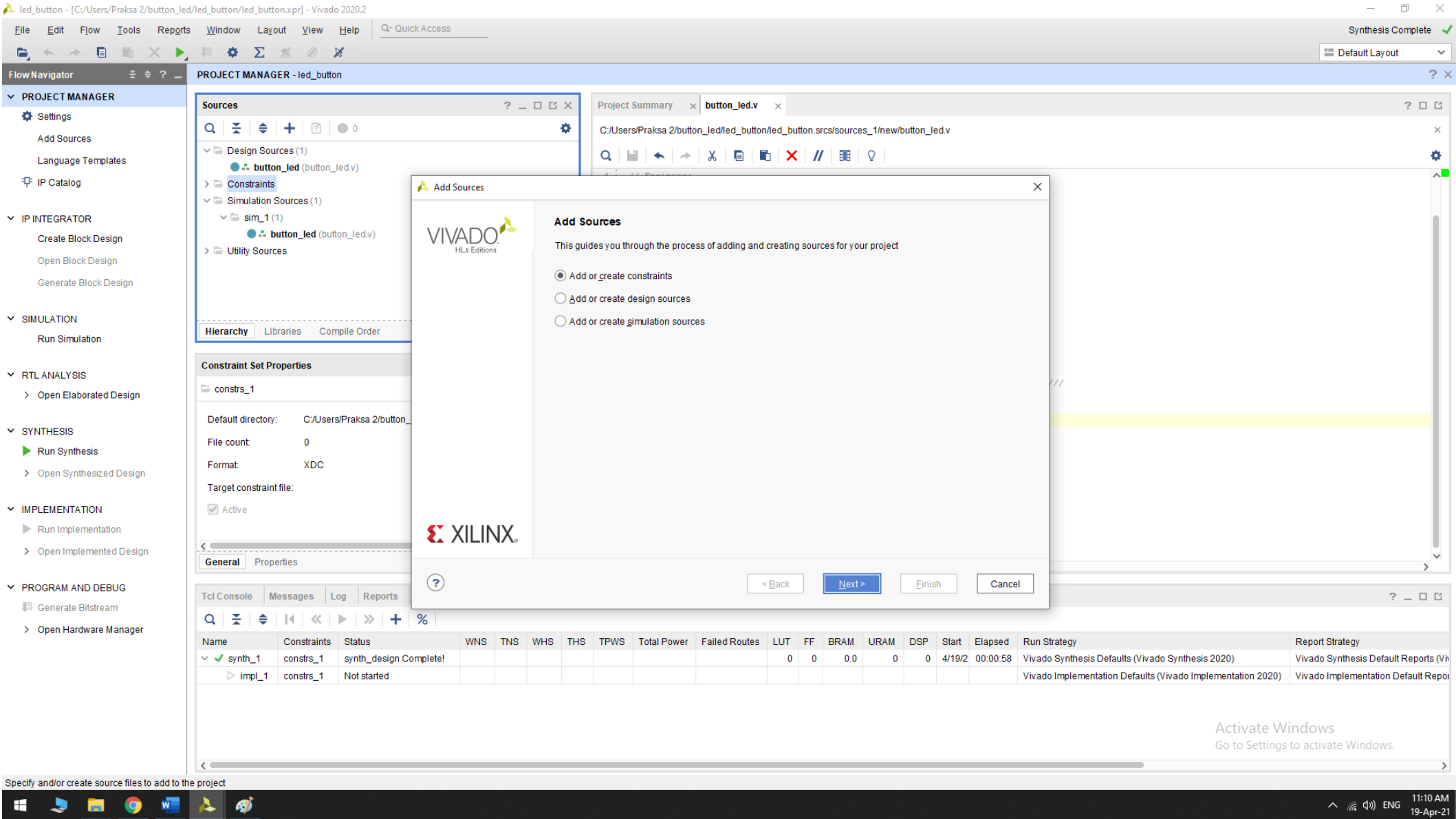
Size: 0.7 KB

Modified: Today at 11:08:43 AM

General Properties

```
Project Summary | button_led.v | button_led_constraints.xdc |  
C:/Users/Praksa 2/button_led/led_button/led_button.srcs/sources_1/new/button_led.v  
4 // Engineer:  
5 //  
6 // Create Date: 04/19/2021 08:49:01 AM  
7 // Design Name:  
8 // Module Name: button_led  
9 // Project Name:  
10 // Target Devices:  
11 // Tool Versions:  
12 // Description:  
13 //  
14 // Dependencies:  
15 //  
16 // Revision:  
17 // Revision 0.01 - File Created  
18 // Additional Comments:  
19 //  
20 ///////////////////////////////////////////////////////////////////  
21  
22  
23 module button_led(input button0, input button1, input button2, input button3,  
24 output led0, output led1, output led2, output led3 );  
25  
26 assign led0 = button0;  
27 assign led1 = button1;  
28 assign led2 = button2;  
29 assign led3 = button3;  
30  
31  
32 endmodule  
33
```

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
------	-------------	--------	-----	-----	-----	-----	------	-------------	---------------	-----	----	------	------	-----	-------	---------	--------------	-----------------



U „Add sources“ biramo „Add or create constraints“ i klinknemo „Next“

The screenshot shows the Vivado 2020.2 interface. The 'Add Sources' dialog box is open, and the 'Add or Create Constraints' sub-dialog is active. The 'Create Constraints File' dialog is also open, showing the file type 'XDC' and the file name 'button\_led\_constraints'. The 'Add Files' button is highlighted.

The 'Add or Create Constraints' dialog has the following fields:

- Specify constraint set: `constrs_1 (active)`
- Buttons: `+ - ↑ ↓`
- Buttons: `Add Files` and `Create File`
- Checkbox:  Copy constraints files into project

The 'Create Constraints File' dialog has the following fields:

- File type: `XDC`
- File name: `button_led_constraints`
- File location: `<Local to Project>`
- Buttons: `OK` and `Cancel`

The background shows the 'PROJECT MANAGER' window with the 'Sources' tree view. The 'Design Sources' section contains 'button\_led (button\_led.v)'. The 'Simulation Sources' section contains 'sim\_1 (1)' and 'button\_led (button\_led.v)'. The 'Utility Sources' section is empty.

The 'Constraint Set Properties' window shows the following details for 'constrs\_1':

- Default directory: `C:/Users/Praksa 2/button_led/button_led.v`
- File count: `0`
- Format: `XDC`
- Target constraint file:  Active

The 'Tcl Console' window shows the following output:

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
✓ synth_1	constrs_1	synth_design Complete!								0	0	0.0	0	0	4/19/2	00:00:58	Vivado Synthesis Defaults (Vivado Synthesis 2020)	Vivado Synthesis Default Reports (Vivado Synthesis 2020)
▷ impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2020)	Vivado Implementation Default Reports (Vivado Implementation 2020)

Activate Windows  
Go to Settings to activate Windows.

Specify and/or create source files to add to the project

11:11 AM  
19-Apr-21



# Definisemo pinove

The screenshot displays the Vivado 2020.2 IDE interface. The top menu bar includes File, Edit, Flow, Tools, Reports, Window, Layout, View, and Help. The main workspace is divided into several panes:

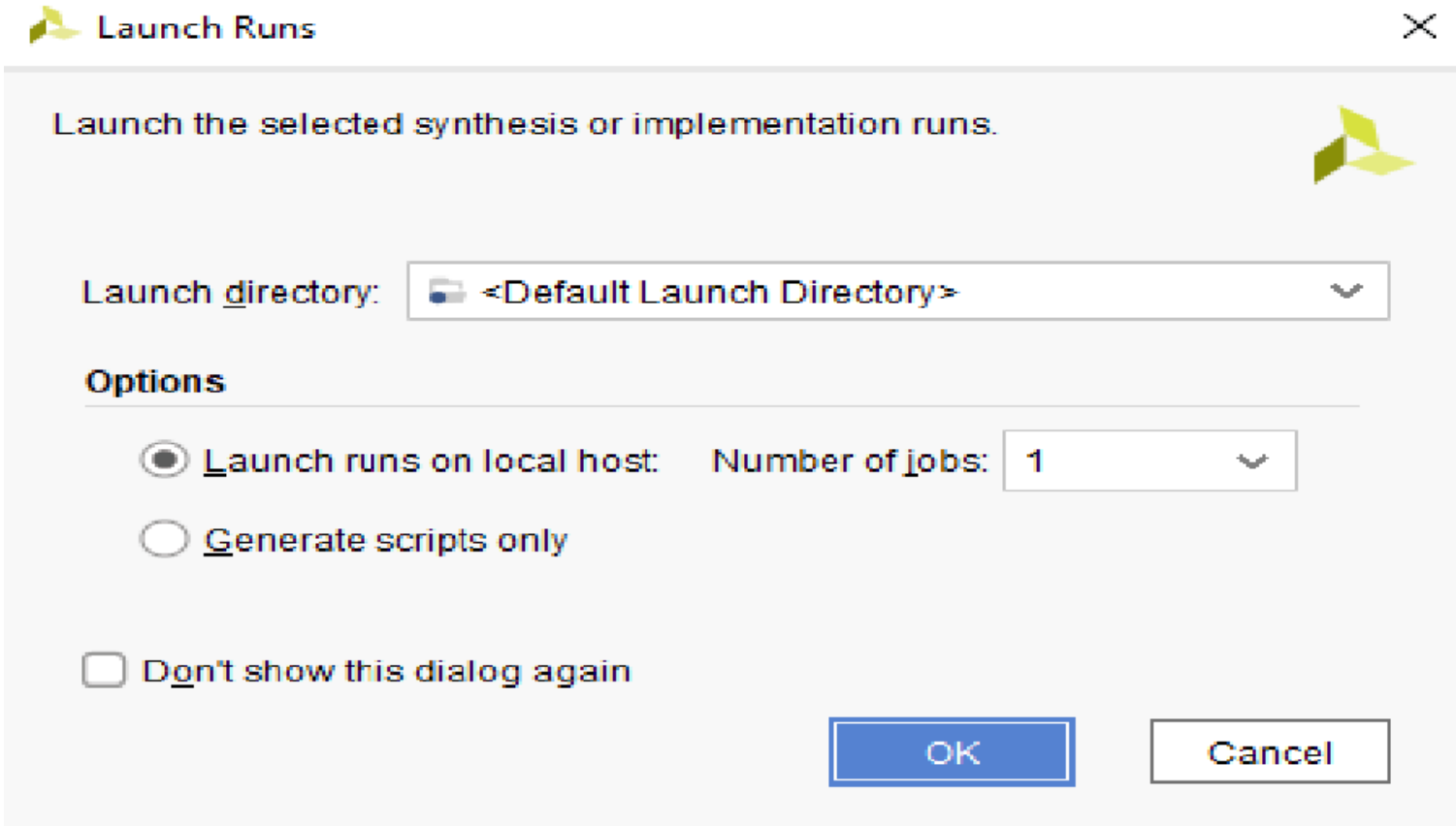
- PROJECT MANAGER - led\_button**: Shows a tree view of sources including Design Sources (button\_led), Constraints (consts\_1), and Simulation Sources.
- Constraint Set Properties**: Shows details for the 'consts\_1' constraint set, including the default directory, file count (1), format (XDC), and target constraint file.
- button\_led\_constraints.xdc**: A text editor showing the following XDC code:

```
1: ##led
2: set_property -dict {PACKAGE_PIN X14 IOSTANDARD LVCMOS33} [get_ports { led0 }];
3: set_property -dict {PACKAGE_PIN F14 IOSTANDARD LVCMOS33} [get_ports { led1 }];
4: set_property -dict {PACKAGE_PIN J16 IOSTANDARD LVCMOS33} [get_ports { led2 }];
5: set_property -dict {PACKAGE_PIN M14 IOSTANDARD LVCMOS33} [get_ports { led3 }];
6:
7: ##push button
8: set_property -dict {PACKAGE_PIN D19 IOSTANDARD LVCMOS33} [get_ports { button0 }];
9: set_property -dict {PACKAGE_PIN D20 IOSTANDARD LVCMOS33} [get_ports { button1 }];
10: set_property -dict {PACKAGE_PIN L20 IOSTANDARD LVCMOS33} [get_ports { button2 }];
11: set_property -dict {PACKAGE_PIN L19 IOSTANDARD LVCMOS33} [get_ports { button3 }];
```
- Tcl Console**: Shows a table of design runs.


Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	consts_1	Synthesis Out-of-date								0	0	0.0	0	0	4/19/21, 11:08 AM	00:00:58	Vivado Synthesis Defaults (Vivado Synthesis 2020)	Vivado Synthesis Defau
impl_1	consts_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2020)	Vivado Implementation

At the bottom right, there is an "Activate Windows" watermark: "Activate Windows. Go to Settings to activate Windows."

# Run Synthesis

A dialog box titled "Launch Runs" with a close button (X) in the top right corner. The main text reads "Launch the selected synthesis or implementation runs." followed by a logo. Below this is a "Launch directory:" label and a dropdown menu showing "<Default Launch Directory>". A section titled "Options" contains three items: a selected radio button for "Launch runs on local host:" with a "Number of jobs:" dropdown set to "1"; an unselected radio button for "Generate scripts only"; and an unchecked checkbox for "Don't show this dialog again". At the bottom are "OK" and "Cancel" buttons.

Launch Runs ×

Launch the selected synthesis or implementation runs. 

Launch directory:

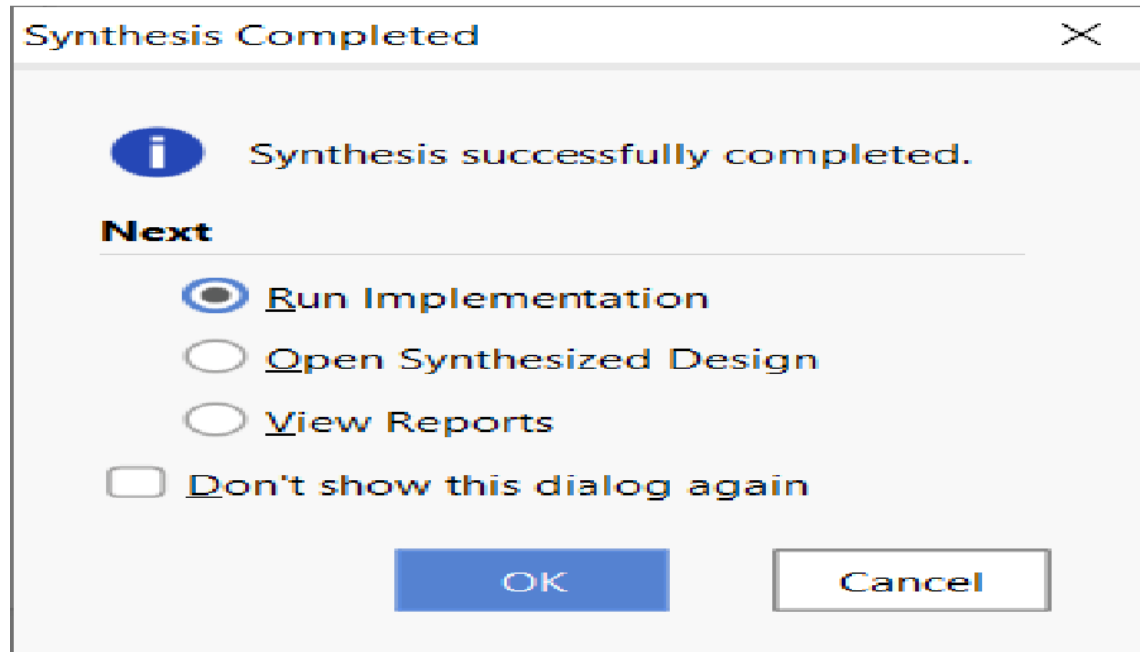
**Options**

Launch runs on local host:    Number of jobs:

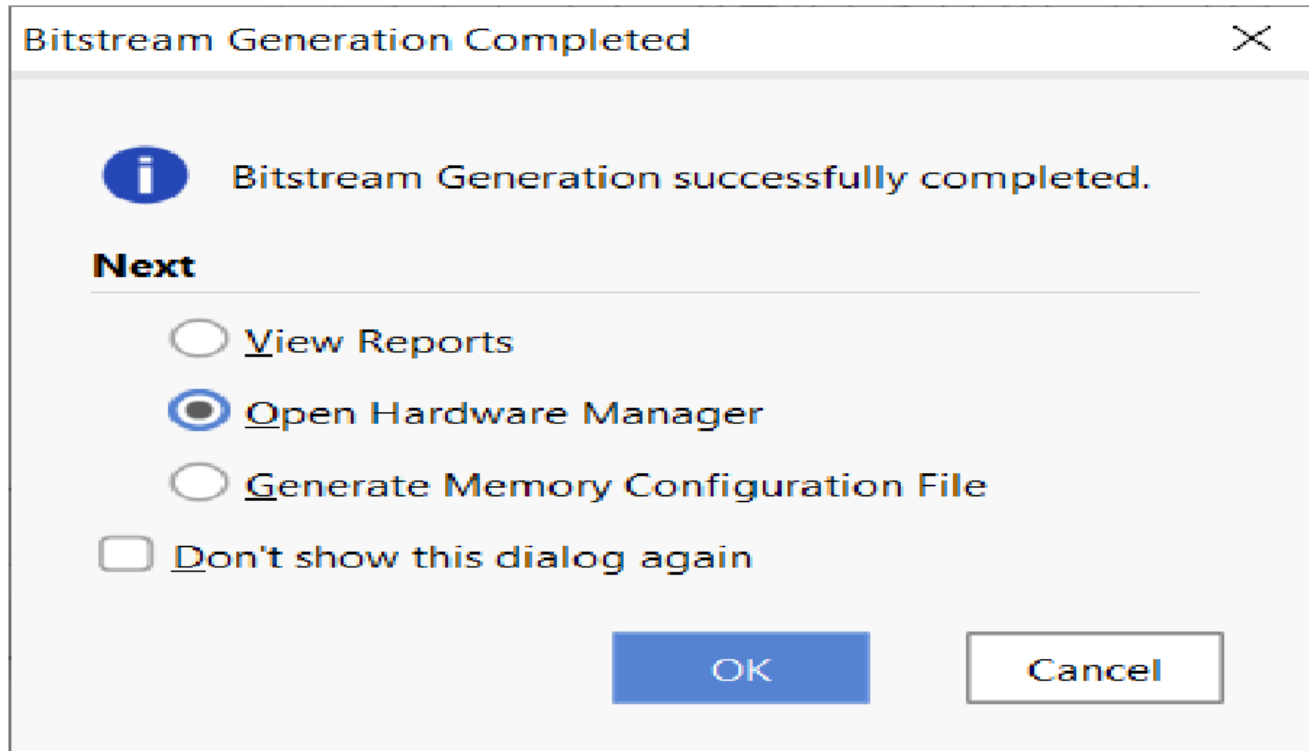
Generate scripts only

Don't show this dialog again

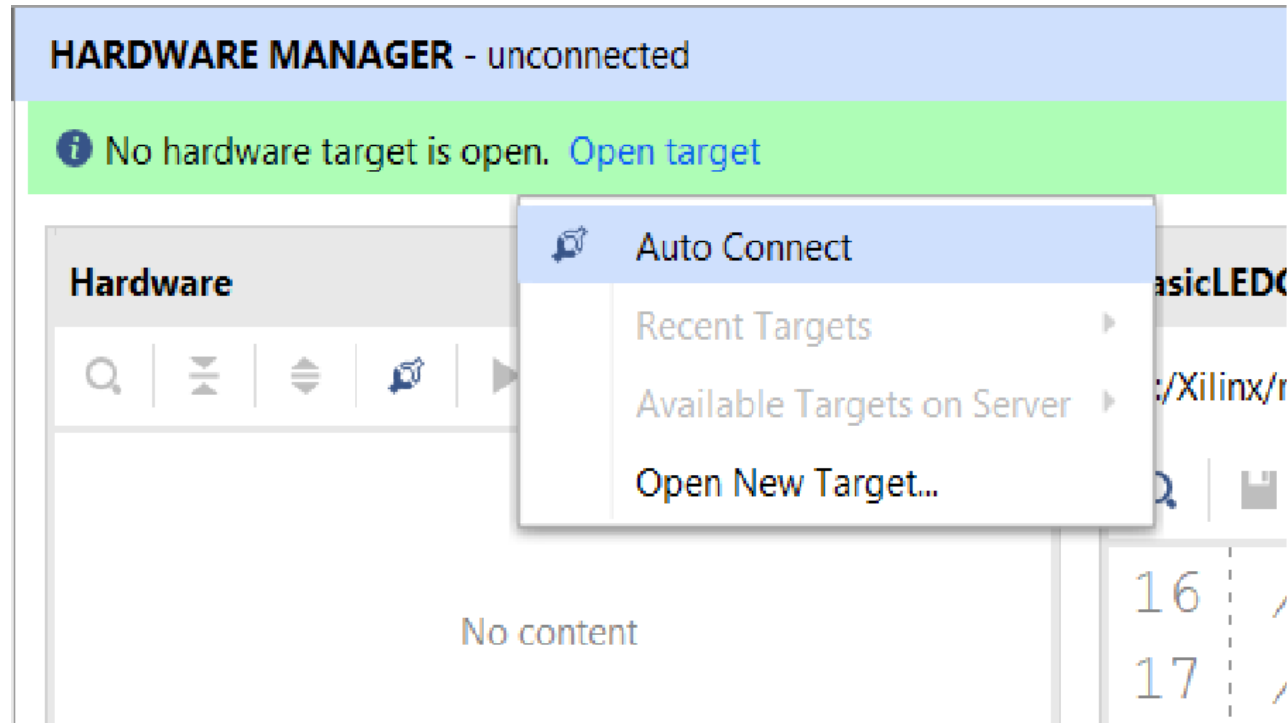
# Run Implementation




# Generisanje Bitstream i programiranje FPGA




# Open target, zatim Auto Connect



# HARDWARE MANAGER - localhost/xilinx\_tcf/Xilinx/1234-tu1A

 No hardware target is open. [Open target](#)









Hardware	
Name	Status
localhost (1)	Connected
 xilinx_tcf/Xilinx/1234-tu1A	Closed

Properties


# HARDWARE MANAGER - localhost/xilinx\_tcf/Xilinx/1234-tula

 There are no debug cores. [Program device](#) [Refresh device](#)

Hardware ? \_ □ ↗ ✕

Name	Status
localhost (1)	Connected
✕ xilinx_tcf/Xilinx/1234-tula (2)	Open
⚙ arm_dap_0 (0)	N/A
✕ ⚙ xc7z020_1 (1)	Not programmed
📊 XADC (System Monitor)	

 Program Device



Select a bitstream programming file and download it to your hardware device. You can optionally select a debug probes file that corresponds to the debug cores contained in the bitstream programming file.



Bitstream file:

'Praksa 2/button\_led/led\_button/led\_button.runs/impl\_1/button\_led.bit' 



Debug probes file:

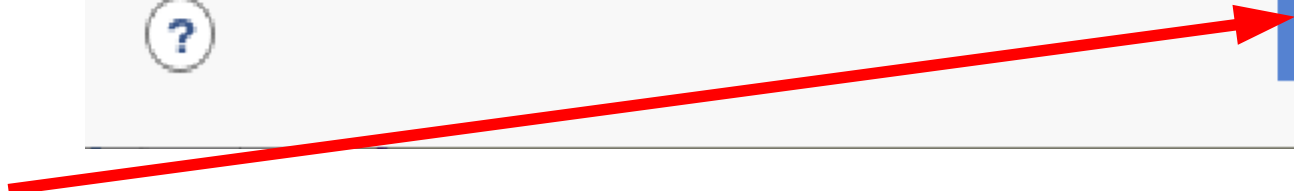


Enable end of startup check



Program

Cancel





Program moze da se testira!  
Klik na taster, ukljucuje se LED!