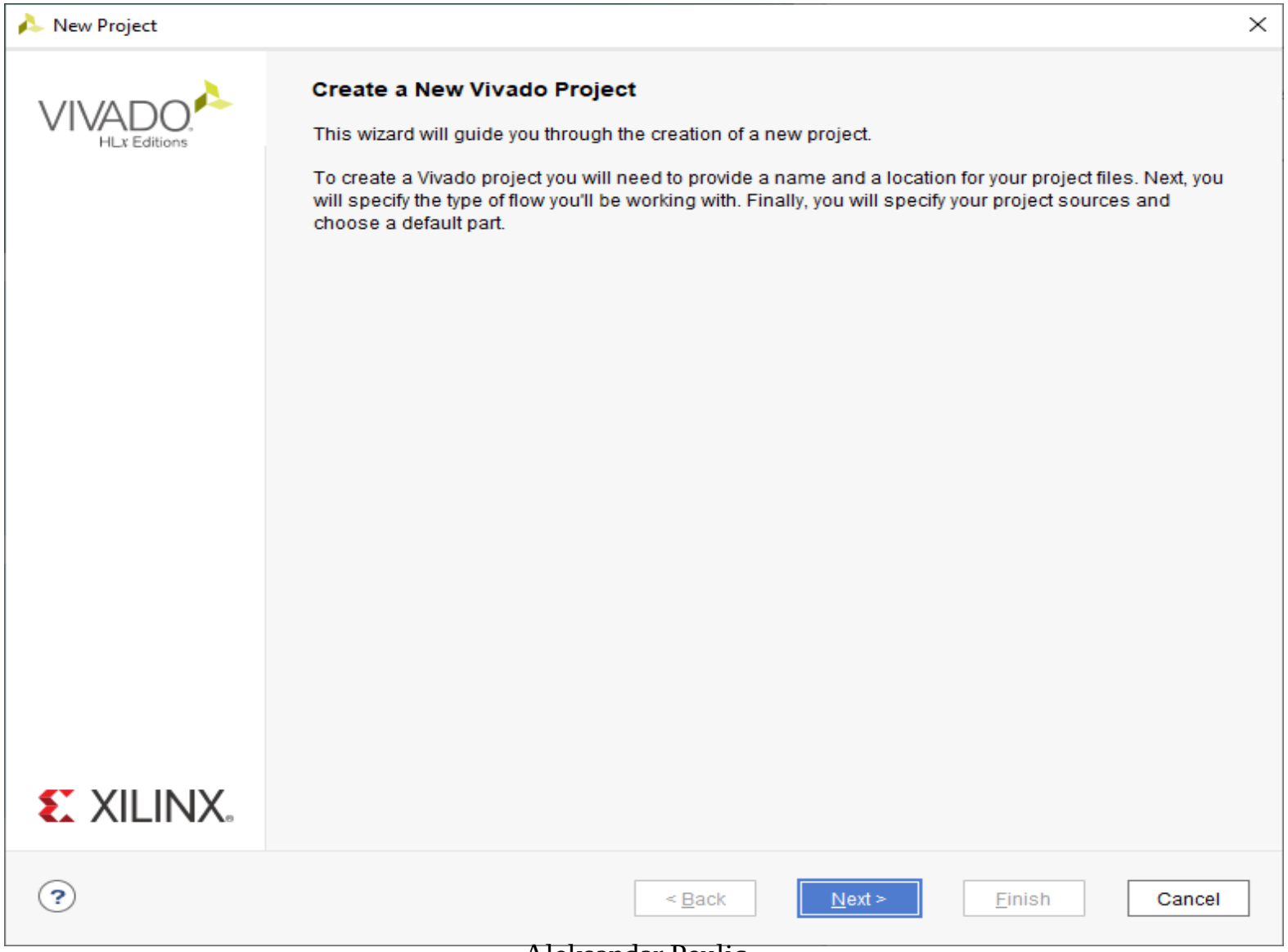
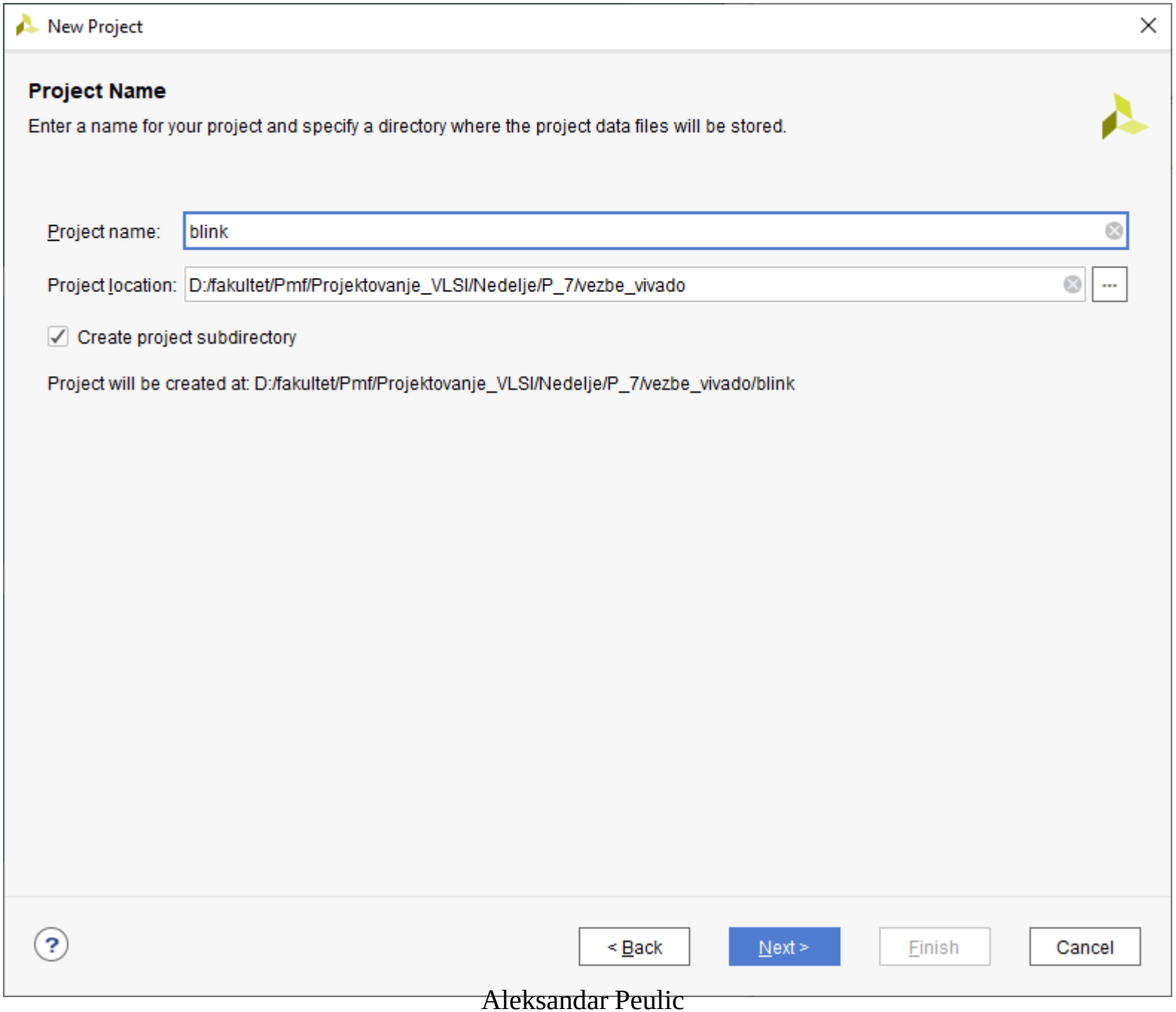
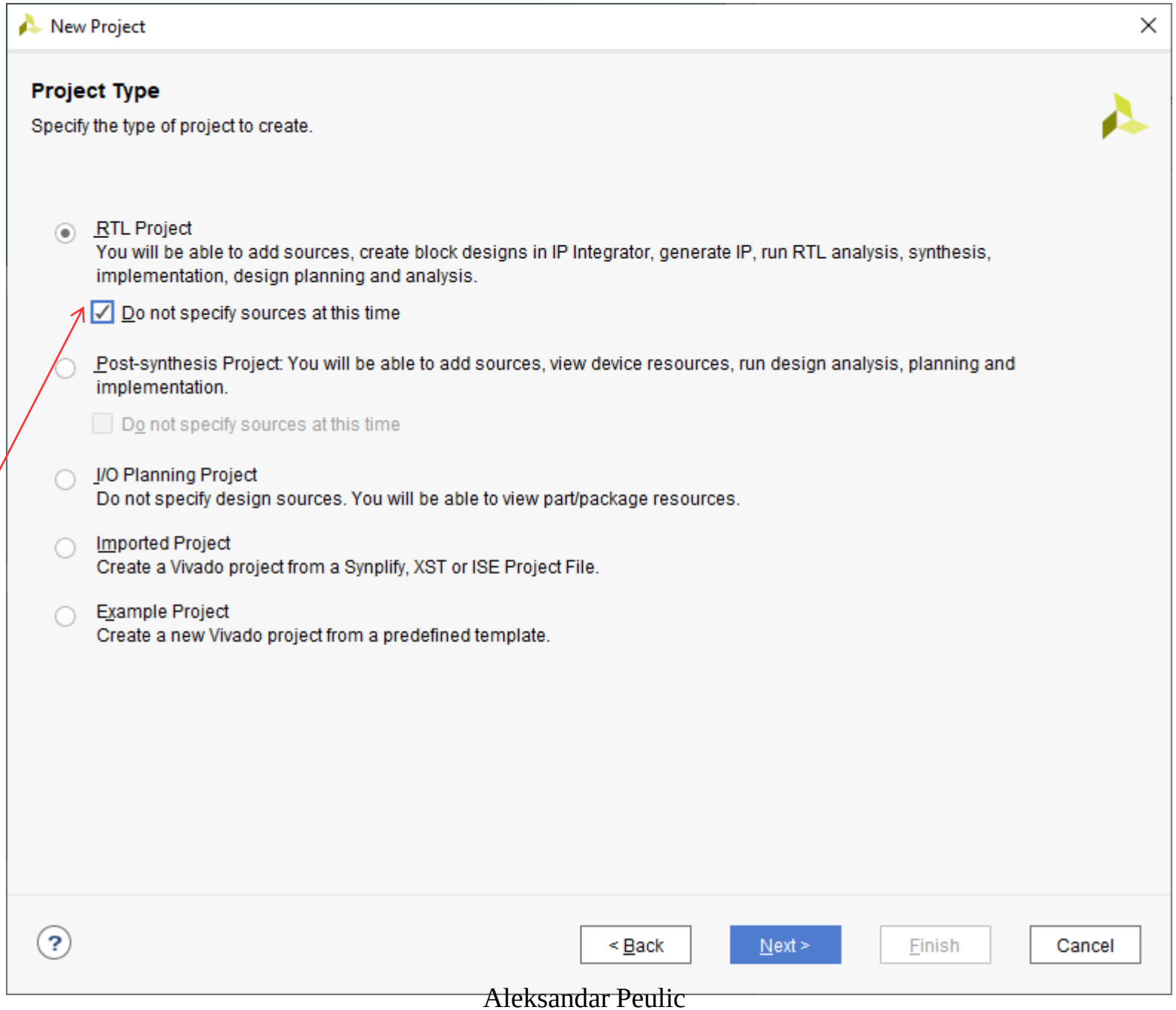
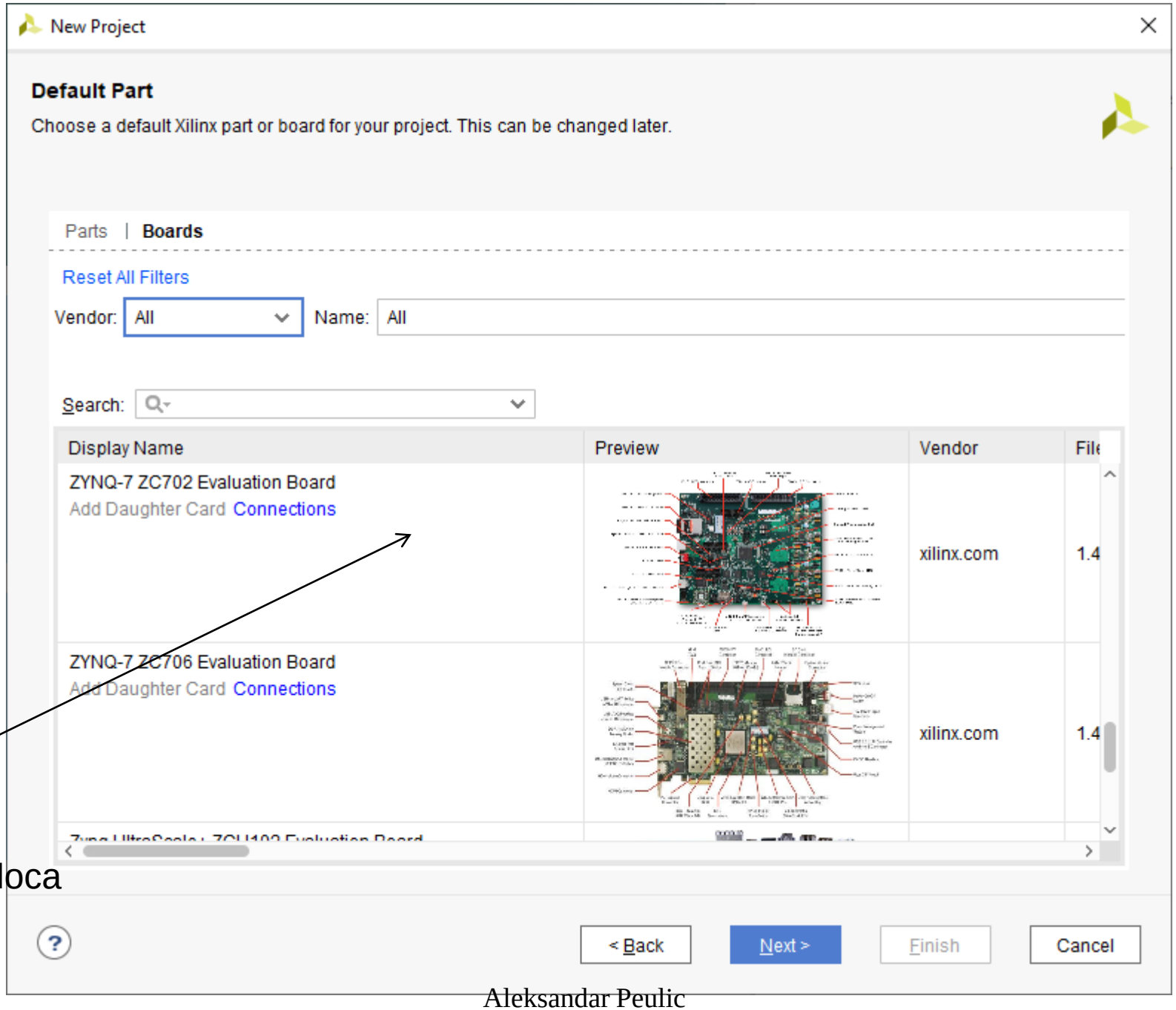
Create New Project

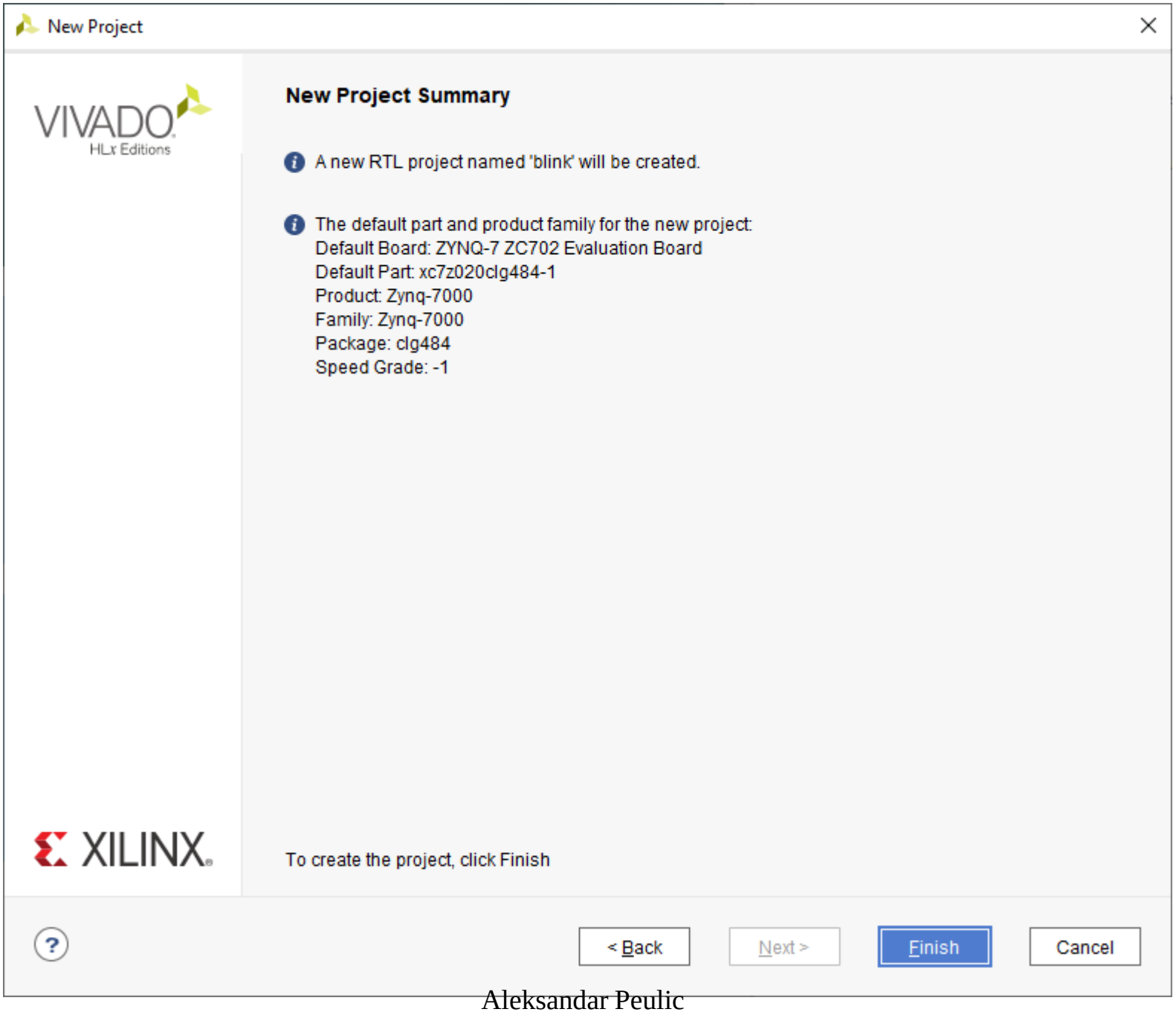


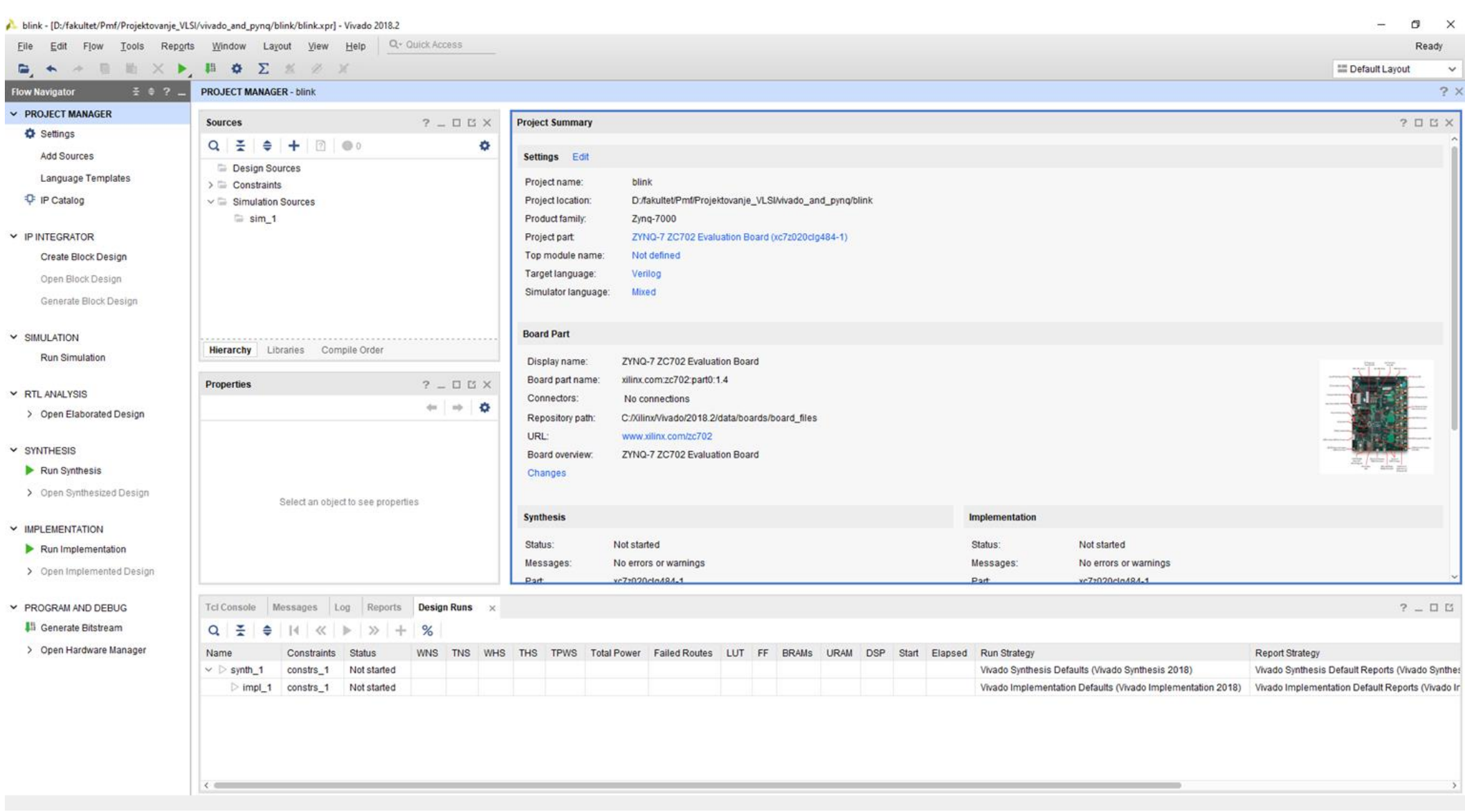

New Project
Project Name
Enter a name for your project and specify a directory where the project data files will be stored.
Project name:
blink
Project location:
D:/fakultet/Pmf/Projektovanje_VLSI/Nedelje/P_7/vezbe_vivado
Create project subdirectory
Project will be created at: D:/fakultet/Pmf/Projektovanje_VLSI/Nedelje/P_7/vezbe_vivado/blink
< Back
Next >
Finish
Cancel


New Project
Project Type
Specify the type of project to create.
RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
Do not specify sources at this time
Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.
Do not specify sources at this time
I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.
Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.
Example Project
Create a new Vivado project from a predefined template.
< Back
Next >
Finish
Cancel



Bira se ploca


New Project
VIVADO
HLx Editions
New Project Summary
A new RTL project named 'blink' will be created.
The default part and product family for the new project:
Default Board: ZYNQ-7 ZC702 Evaluation Board
Default Part: xc7z020clg484-1
Product: Zynq-7000
Family: Zynq-7000
Package: clg484
Speed Grade: -1
XILINX
To create the project, click Finish
< Back
Next >
Finish
Cancel



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4. The Flow Navigator

The *Flow Navigator* is the most important pane of the main Vivado window to know. It is how a user navigates between different Vivado tools.

The Navigator is broken into seven sections:

- *Project Manager*
  - Allows for quick access to project settings, adding sources, language templates, and the IP catalog
- *IP Integrator*
  - Tools for creating Block Designs
- *Simulation*
  - Allows a developer to verify the output of their design prior to programming their device
- *RTL Analysis*
  - lets the developer see how the tools are interpreting their code
- *Synthesis*
  - Gives access to Synthesis settings and post-synthesis reports
- *Implementation*
  - Gives access to Implementation settings and post-implementation reports
- *Program and Debug*
  - Access to settings for bitstream generation and the Hardware Manager

5. The Project Manager

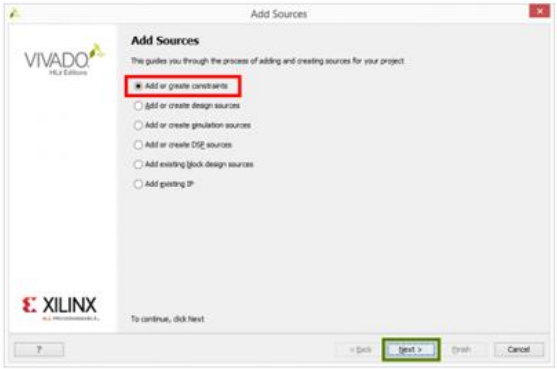
Adding a Constraint File

In order to connect HDL code with the physical pins of the FPGA, a constraint file needs to be added or created. Digilent has produced a Xilinx Design Constraint (XDC) file for each of our boards. Download digilent-xdc-master.zip, the ZIP Archive containing each of these master XDC files, then extract it in a location you will remember.

Dodaje se I bira Costrain file iz Menija Add Source

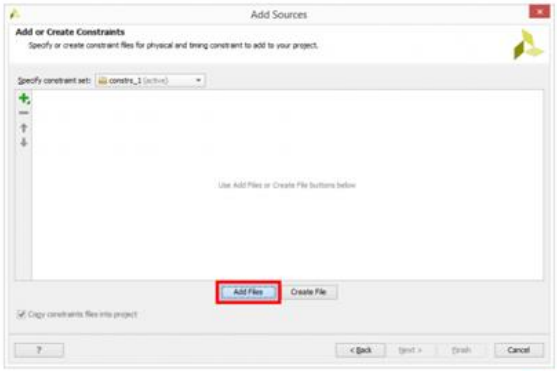
6.1

In the *Project Manager* section of the *Flow Navigator*, click the Add Sources button. In the wizard that pops up, select *Add or create constraints* then click *Next*.



6.2

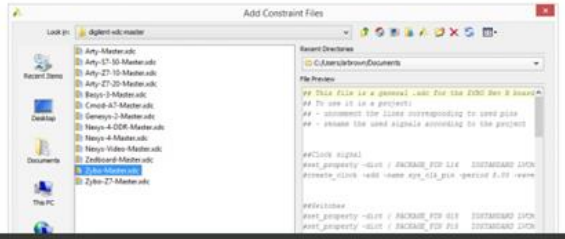
At this stage, Vivado provides a list of all of the constraint files that will be added or created when we click Finish. Currently this list is empty, this will change when files have been added or created. A constraint file will not be created from scratch in this guide, so click *Add Files*.

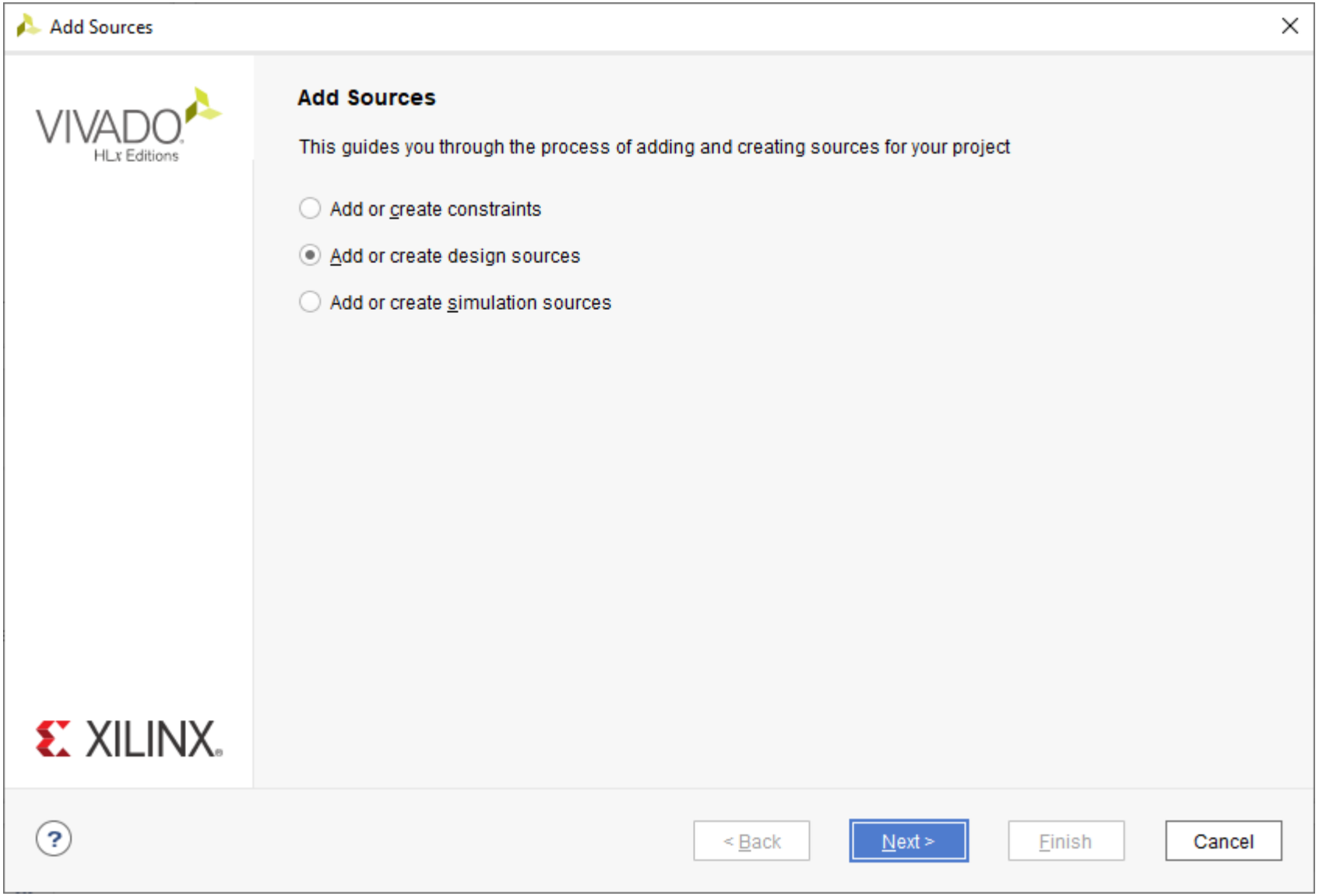


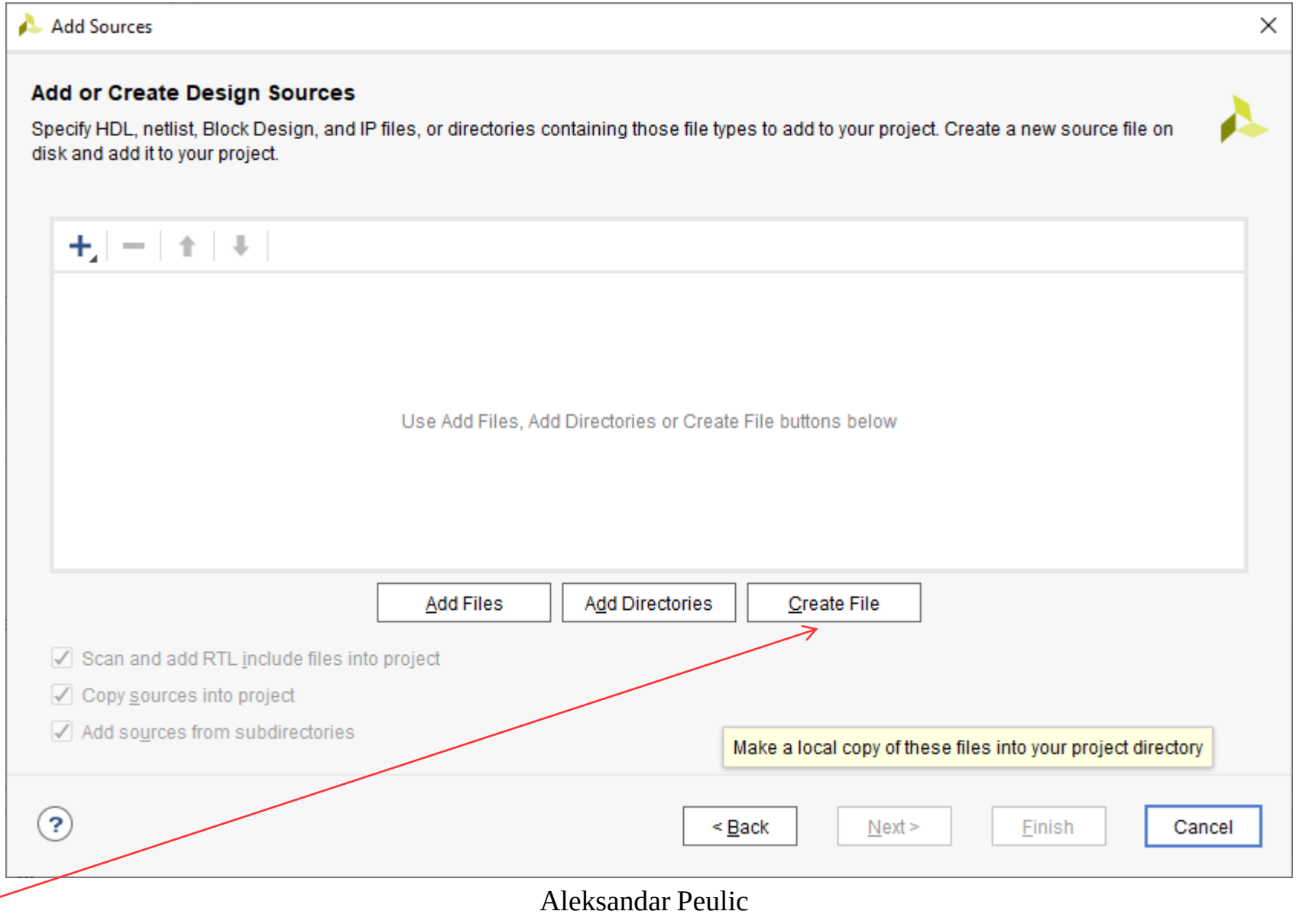
6.3

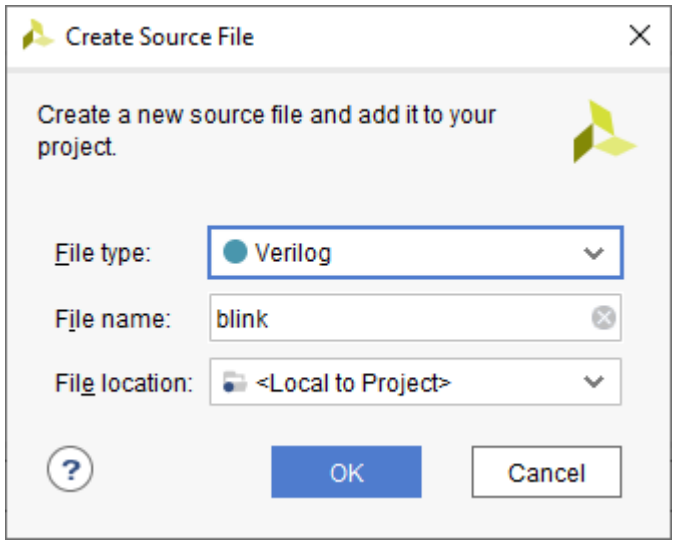
Find the directory you extracted the *digilent-xdc-master.zip* archive into, then click on the file for your board. This should add the name of the file to the *File Name* field.

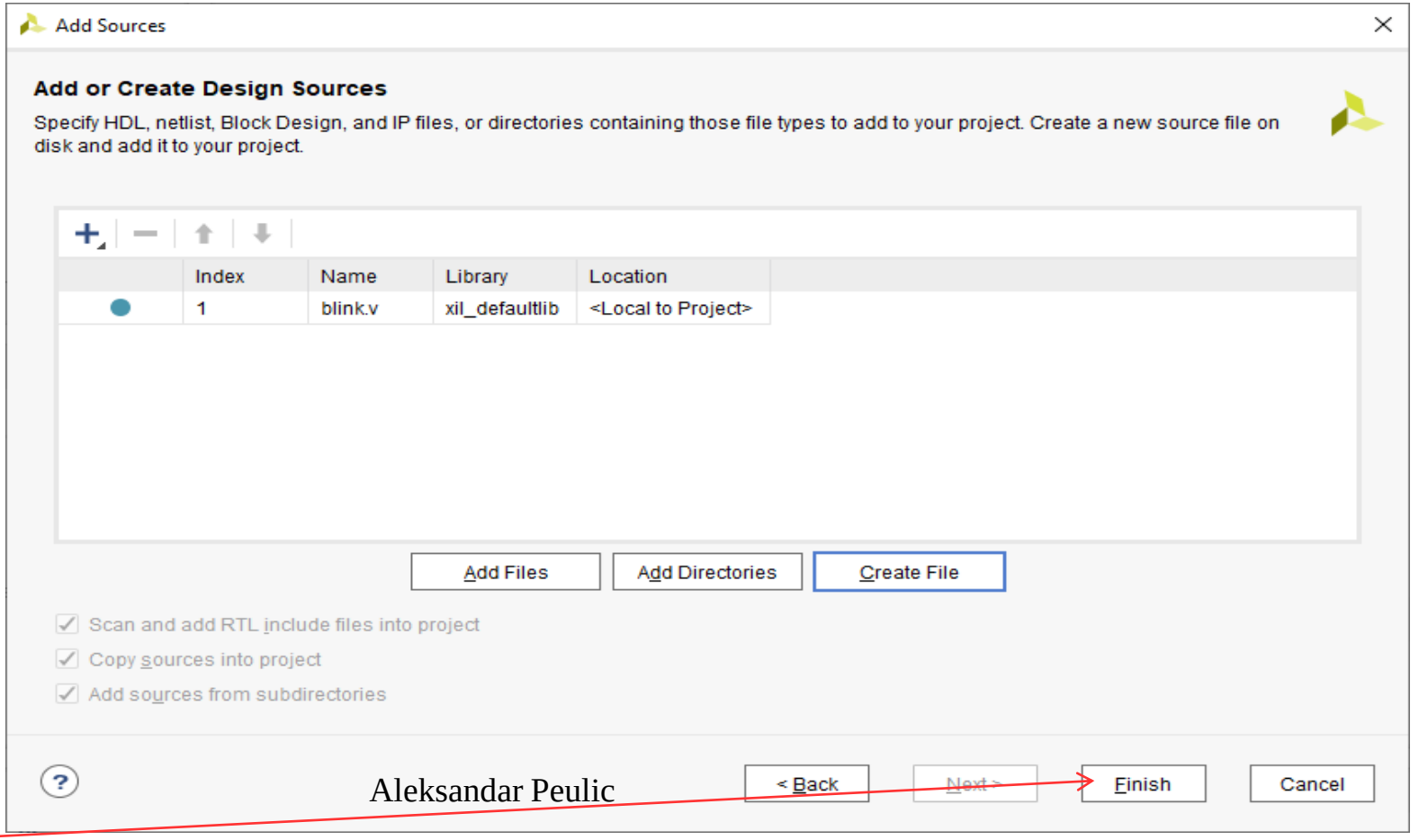
Click *OK* to continue.




Add Sources
VIVADO
HLx Editions
Add Sources
This guides you through the process of adding and creating sources for your project
Add or create constraints
Add or create design sources
Add or create simulation sources
XILINX
< Back
Next >
Finish
Cancel


Add Sources
Add or Create Design Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.
Use Add Files, Add Directories or Create File buttons below
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Make a local copy of these files into your project directory
< Back
Next >
Finish
Cancel





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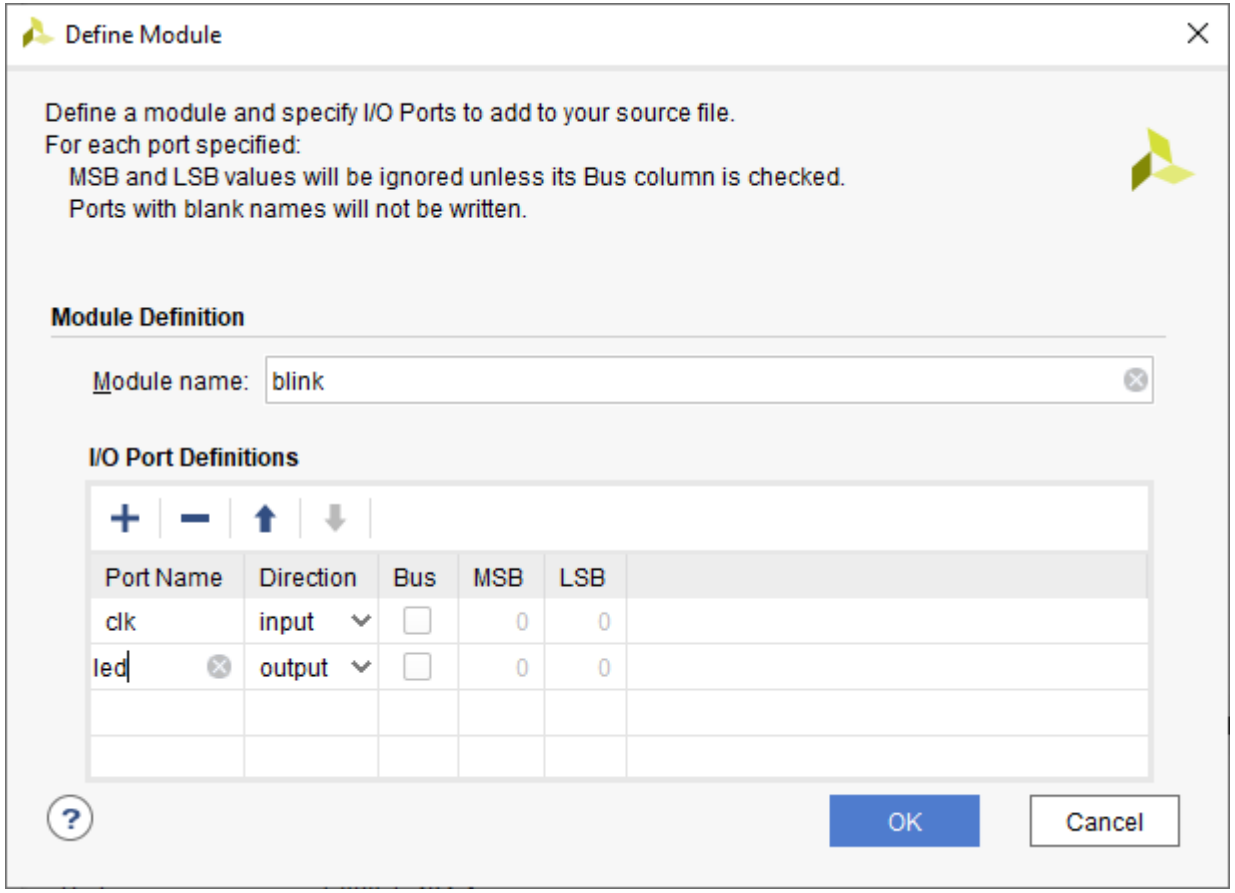
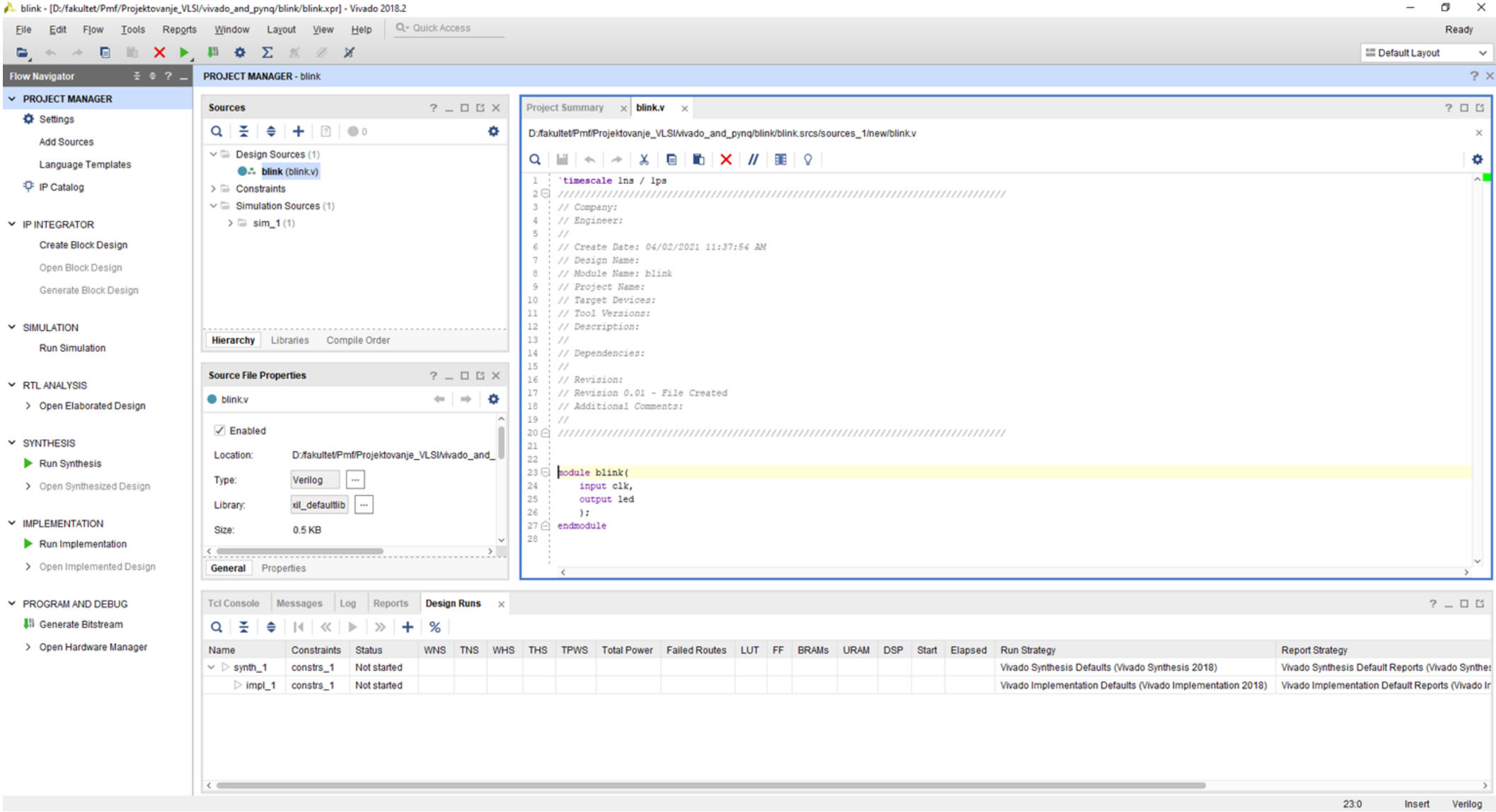

Define Module
Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.
Module Definition
Module name:
blink
I/O Port Definitions
Port Name
Direction
Bus
MSB
LSB
clk
input
0
0
led
output
0
0
OK
Cancel



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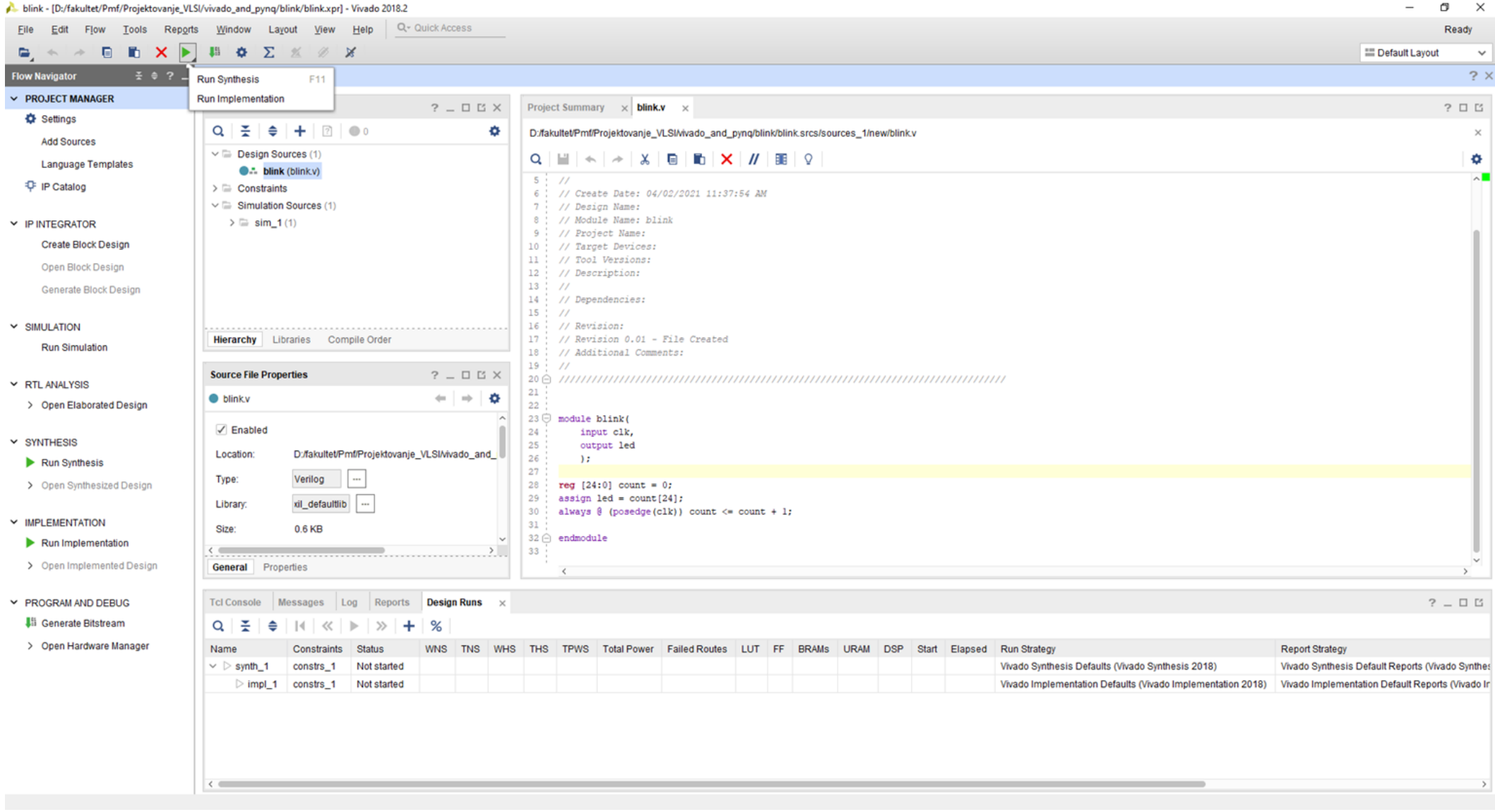

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