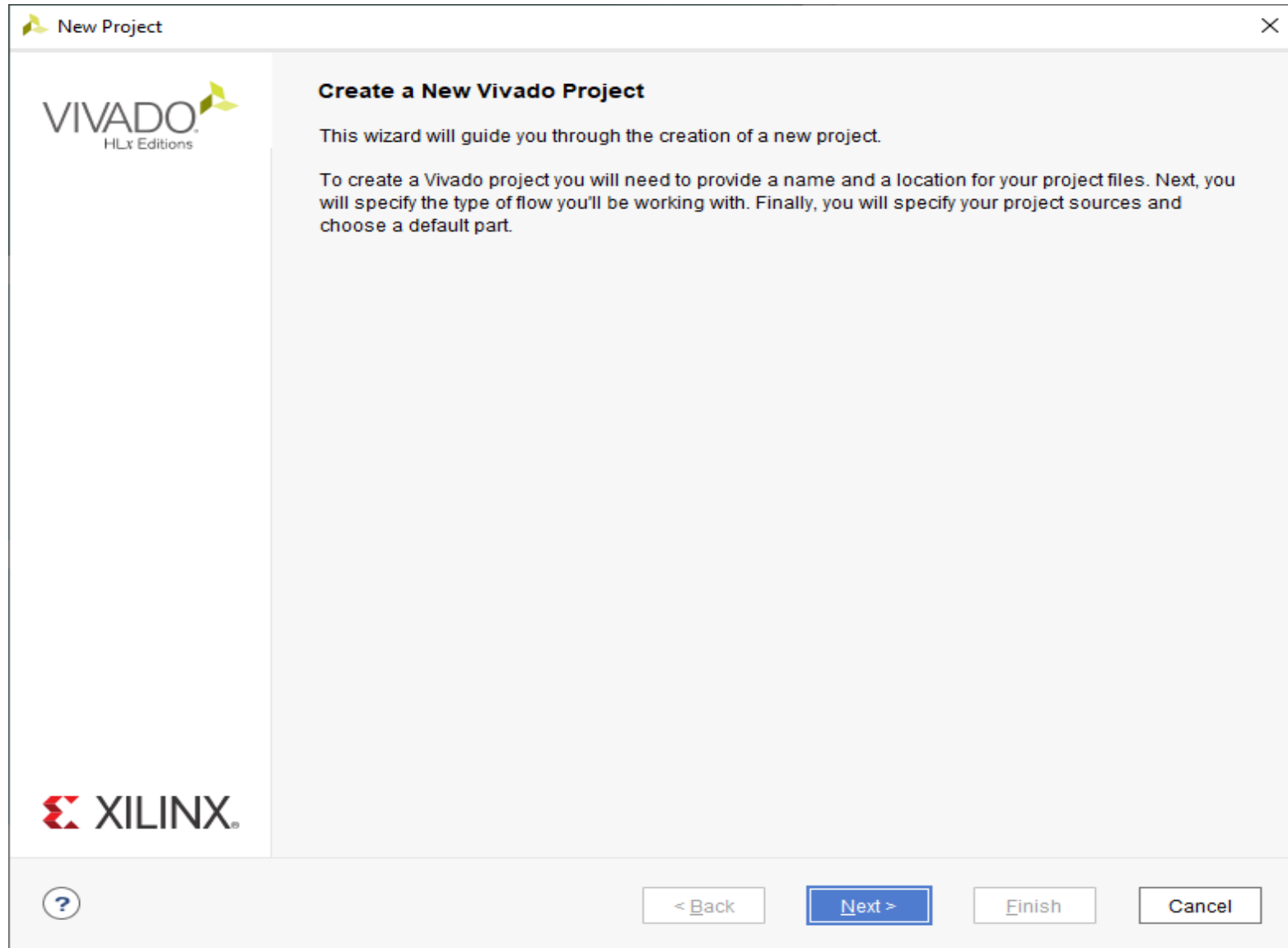



Create New Project



New Project ×

Project Name 

Enter a name for your project and specify a directory where the project data files will be stored.

Project name:


Project location: × ...

Create project subdirectory

Project will be created at: D:/fakultet/Pmf/Projektovanje_VLSI/Nedelje/P_7/vezbe_vivado/blink

?

New Project ×

Project Type 

Specify the type of project to create.

- RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
- Do not specify sources at this time**
- Post-synthesis Project.** You will be able to add sources, view device resources, run design analysis, planning and implementation.
 - Do not specify sources at this time**
- I/O Planning Project**
Do not specify design sources. You will be able to view part/package resources.
- Imported Project**
Create a Vivado project from a Synplify, XST or ISE Project File.
- Example Project**
Create a new Vivado project from a predefined template.

? < Back Next > Finish Cancel

New Project

Default Part

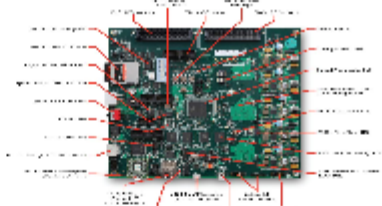
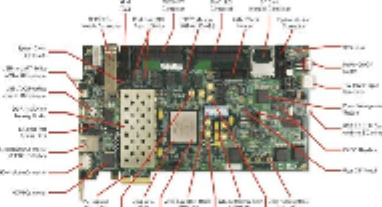

Choose a default Xilinx part or board for your project. This can be changed later.

Parts | **Boards**

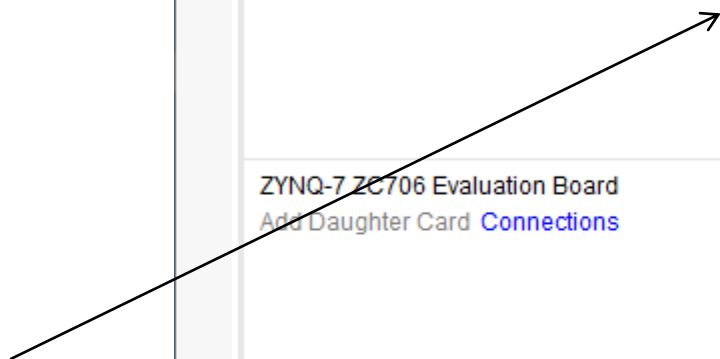
[Reset All Filters](#)

Vendor: Name:

Search:



Display Name	Preview	Vendor	File
ZYNQ-7 ZC702 Evaluation Board Add Daughter Card Connections		xilinx.com	1.4
ZYNQ-7 ZC706 Evaluation Board Add Daughter Card Connections		xilinx.com	1.4
Zynq UltraScale+ ZCU102 Evaluation Board			

[?](#)



Bira se ploca

New Project ×

New Project Summary

- i A new RTL project named 'blink' will be created.

- i The default part and product family for the new project:
Default Board: ZYNQ-7 ZC702 Evaluation Board
Default Part: xc7z020clg484-1
Product: Zynq-7000
Family: Zynq-7000
Package: clg484
Speed Grade: -1

To create the project, click Finish

?< BackNext >FinishCancel

blink - [D:\fakultet\Pmf\Projektovanje_VLSI\vivado_and_pynq\blink\blink.xpr] - Vivado 2018.2

File Edit Flow Tools Reports Window Layout View Help Quick Access

Flow Navigator PROJECT MANAGER - blink

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog
- IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION
 - Run Simulation
- RTL ANALYSIS
 - Open Elaborated Design
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
- PROGRAM AND DEBUG
 - Generate Bitstream
 - Open Hardware Manager

Sources

- Design Sources
- Constraints
- Simulation Sources
 - sim_1

Hierarchy Libraries Compile Order

Properties

Select an object to see properties

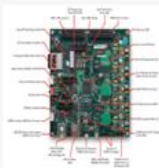
Project Summary

Settings Edit

Project name: blink
 Project location: D:\fakultet\Pmf\Projektovanje_VLSI\vivado_and_pynq\blink
 Product family: Zynq-7000
 Project part: ZYNQ-7 ZC702 Evaluation Board (xc7z020clg484-1)
 Top module name: Not defined
 Target language: Verilog
 Simulator language: Mixed

Board Part

Display name: ZYNQ-7 ZC702 Evaluation Board
 Board part name: xilinx.com:zc702:part0:1.4
 Connectors: No connections
 Repository path: C:\Xilinx\Vivado\2018.2\data\boards\board_files
 URL: www.xilinx.com/xc7z020
 Board overview: ZYNQ-7 ZC702 Evaluation Board
[Changes](#)



Synthesis Implementation

Status: Not started
 Messages: No errors or warnings
 Part: xc7z020clg484-1

Tcl Console Messages Log Reports Design Runs

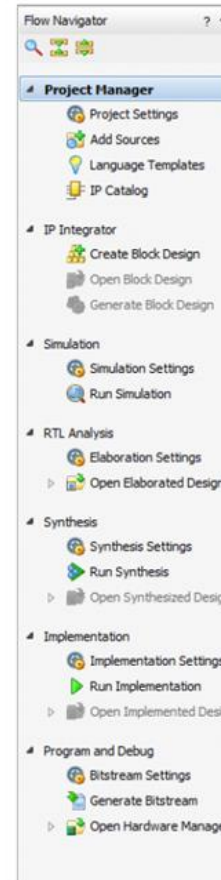
Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2018)	Vivado Synthesis Default Reports (Vivado Synthesis 2018)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2018)	Vivado Implementation Default Reports (Vivado Implementation 2018)

4. The Flow Navigator

The *Flow Navigator* is the most important pane of the main Vivado window to know. It is how a user navigates between different Vivado tools.

The Navigator is broken into seven sections:

- **Project Manager**
 - Allows for quick access to project settings, adding sources, language templates, and the IP catalog
- **IP Integrator**
 - Tools for creating Block Designs
- **Simulation**
 - Allows a developer to verify the output of their design prior to programming their device
- **RTL Analysis**
 - lets the developer see how the tools are interpreting their code
- **Synthesis**
 - Gives access to Synthesis settings and post-synthesis reports
- **Implementation**
 - Gives access to Implementation settings and post-implementation reports
- **Program and Debug**
 - Access to settings for bitstream generation and the Hardware Manager



5. The Project Manager

Adding a Constraint File

In order to connect HDL code with the physical pins of the FPGA, a constraint file needs to be added or created. Digilent has produced a Xilinx Design Constraint (XDC) file for each of our boards. Download digilent-xdc-master.zip, the ZIP Archive containing each of these master XDC files, then extract it in a location you will remember.

Dodaje se I bira Costrain file iz Menija Add Source

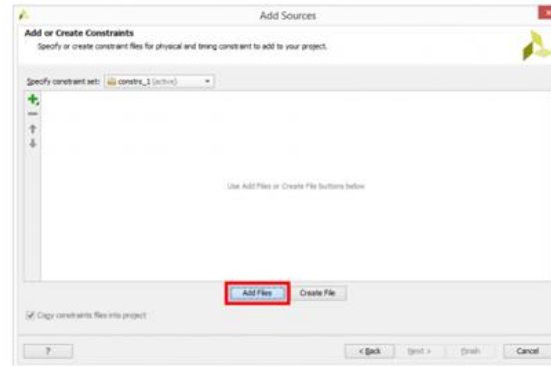
6.1

In the *Project Manager* section of the *Flow Navigator*, click the **Add Sources** button. In the wizard that pops up, select **Add or create constraints** then click **Next**.



6.2

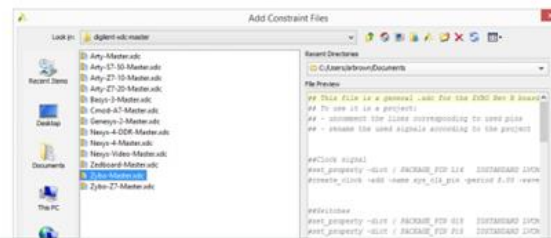
At this stage, Vivado provides a list of all of the constraint files that will be added or created when we click Finish. Currently this list is empty, this will change when files have been added or created. A constraint file will not be created from scratch in this guide, so click **Add Files**.

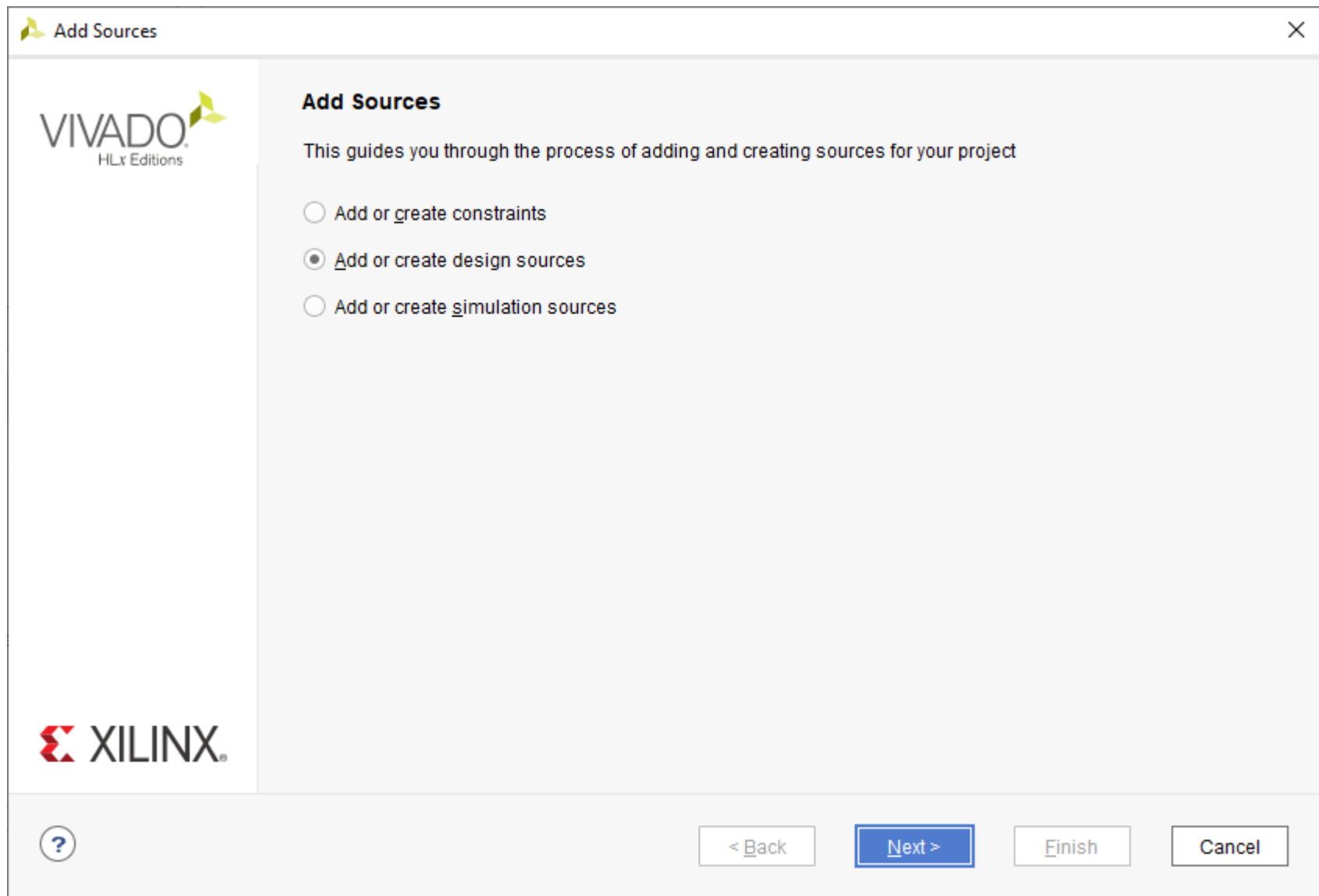


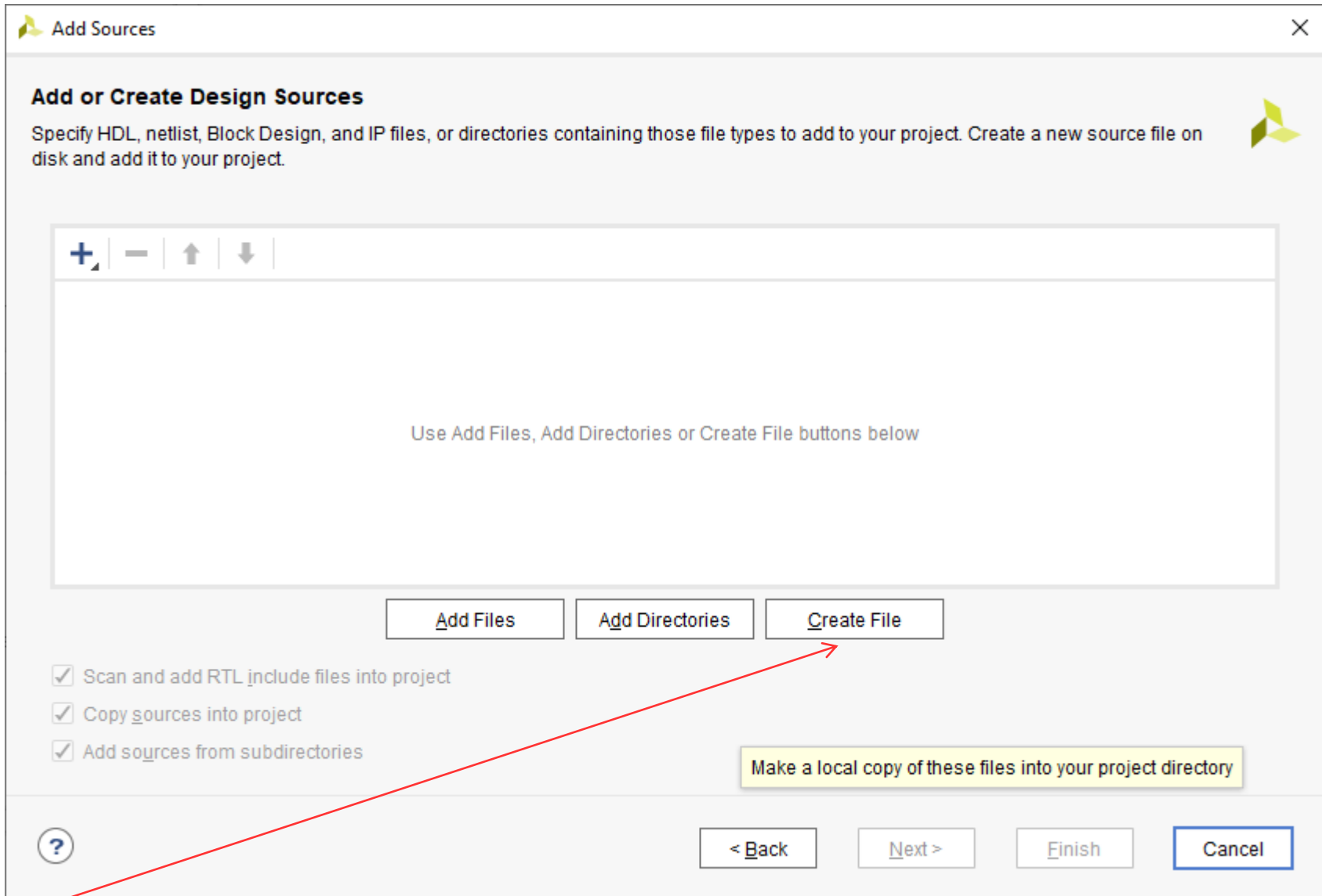
6.3

Find the directory you extracted the *digilent-xdc-master.zip* archive into, then click on the file for your board. This should add the name of the file to the *File Name* field.

Click **OK** to continue.







Create Source File

Create a new source file and add it to your project.

File type: Verilog

File name: blink

File location: <Local to Project>

OK Cancel

Add Sources

Add or Create Design Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.

	Index	Name	Library	Location
●	1	blink.v	xil_defaultlib	<Local to Project>

Add Files Add Directories Create File

Scan and add RTL include files into project
 Copy sources into project
 Add sources from subdirectories

Aleksandar Peulic < Back Next > Finish Cancel

Define Module

Define a module and specify I/O Ports to add to your source file.
 For each port specified:
 MSB and LSB values will be ignored unless its Bus column is checked.
 Ports with blank names will not be written.

Module Definition

Module name:

I/O Port Definitions

Port Name	Direction	Bus	MSB	LSB
clk	input	<input type="checkbox"/>	0	0
led	output	<input type="checkbox"/>	0	0

blink - [D:/fakultet/Pmf/Projektovanje_VLSI/vivado_and_pynq/blink/blink.xpr] - Vivado 2018.2

File Edit Flow Tools Reports Window Layout View Help Quick Access

Flow Navigator PROJECT MANAGER - blink

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog
- IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION
 - Run Simulation
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 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
- PROGRAM AND DEBUG
 - Generate Bitstream
 - Open Hardware Manager

Sources

- Design Sources (1)
 - blink (blink.v)
- Constraints
- Simulation Sources (1)
 - sim_1 (1)

Hierarchy Libraries Compile Order

Source File Properties

blink.v

- Enabled
- Location: D:/fakultet/Pmf/Projektovanje_VLSI/vivado_and_
- Type: Verilog
- Library: xil_defaultlib
- Size: 0.5 KB

General Properties

Project Summary x blink.v x

D:/fakultet/Pmf/Projektovanje_VLSI/vivado_and_pynq/blink/blink.srcs/sources_1/new/blink.v

```

1 `timescale 1ns / 1ps
2 //////////////////////////////////////////////////
3 // Company:
4 // Engineer:
5 //
6 // Create Date: 04/02/2021 11:37:54 AM
7 // Design Name:
8 // Module Name: blink
9 // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////
21
22
23 module blink(
24     input clk,
25     output led
26 );
27 endmodule
28

```

Tcl Console Messages Log Reports Design Runs x

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2018)	Vivado Synthesis Default Reports (Vivado Synthesis 2018)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2018)	Vivado Implementation Default Reports (Vivado Implementation 2018)

23.0 Insert Verilog

blink - [D:/fakultet/Pmf/Projektovanje_VLSI/vivado_and_pynq/blink/blink.xpr] - Vivado 2018.2

File Edit Flow Tools Reports Window Layout View Help Q- Quick Access Ready

Flow Navigator Run Synthesis F11 Run Implementation

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Design Sources (1)

- blink (blink.v)

Constraints

Simulation Sources (1)

- sim_1 (1)

Hierarchy Libraries Compile Order

Source File Properties

blink.v

- Enabled

Location: D:/fakultet/Pmf/Projektovanje_VLSI/vivado_and_pynq/blink/srcs/sources_1/new/blink.v

Type: Verilog

Library: xil_defaultlib

Size: 0.6 KB

General Properties

Project Summary x blink.v x

D:/fakultet/Pmf/Projektovanje_VLSI/vivado_and_pynq/blink/srcs/sources_1/new/blink.v

```

5 //
6 // Create Date: 04/02/2021 11:37:54 AM
7 // Design Name:
8 // Module Name: blink
9 // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21 //
22 //
23 module blink(
24     input clk,
25     output led
26 );
27
28 reg [24:0] count = 0;
29 assign led = count[24];
30 always @ (posedge(clk)) count <= count + 1;
31
32 endmodule
33

```

Tcl Console Messages Log Reports Design Runs x

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2018)	Vivado Synthesis Default Reports (Vivado Synthesis 2018)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2018)	Vivado Implementation Default Reports (Vivado Implementation 2018)