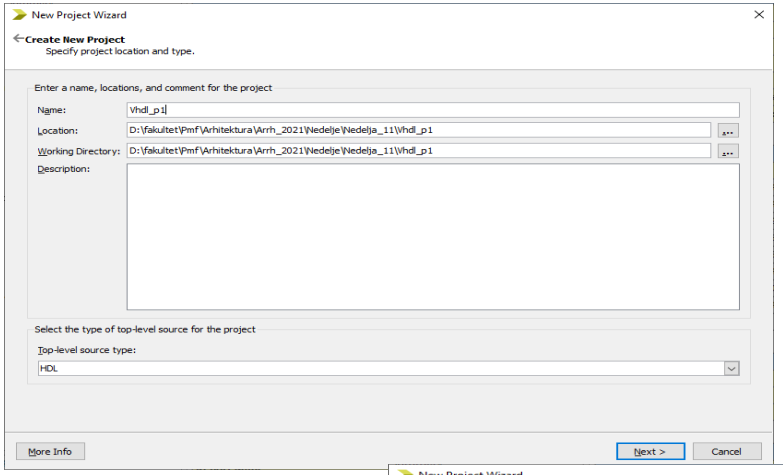
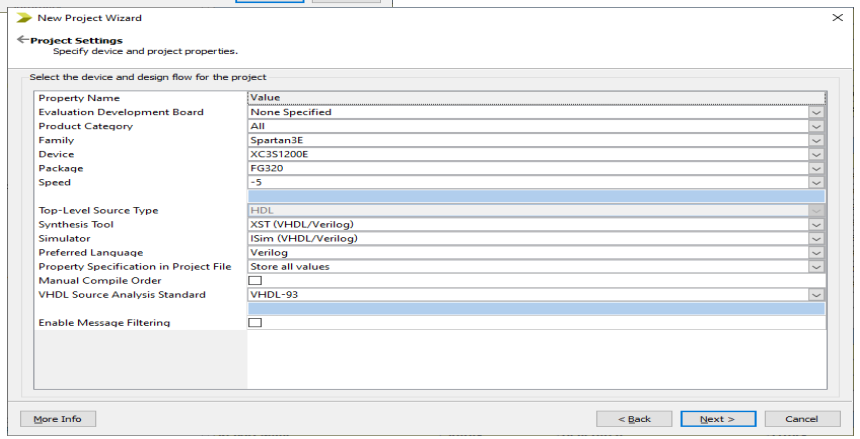
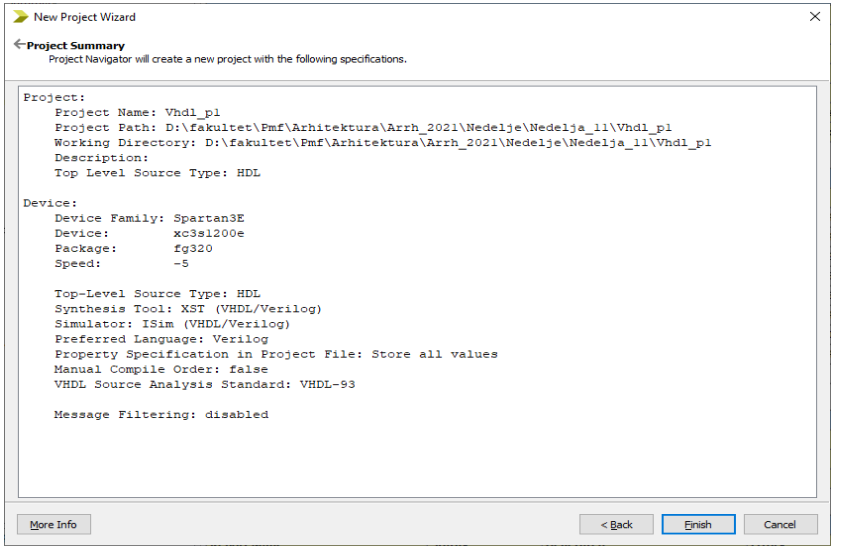
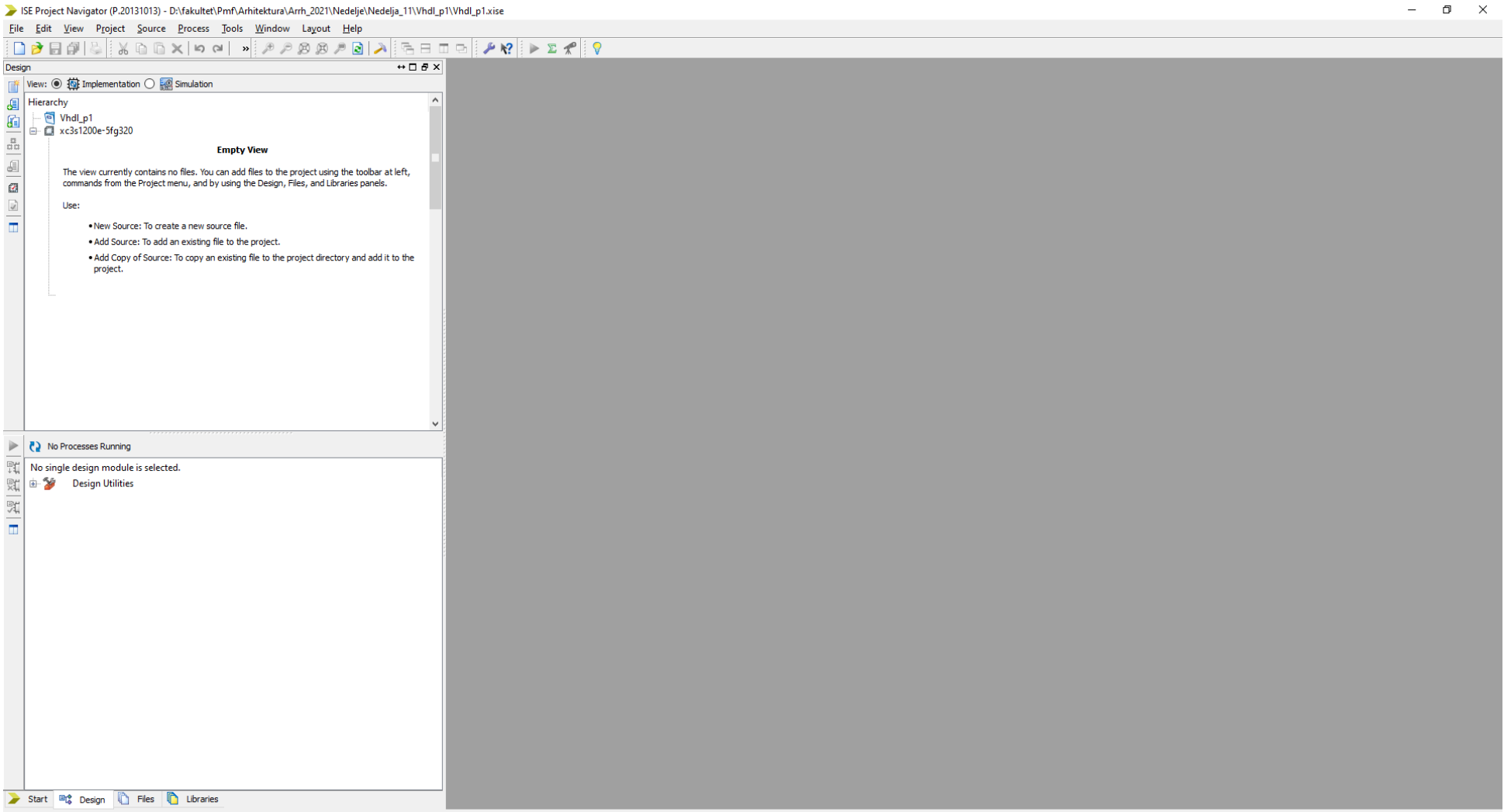
VHDL primeri Xilinx

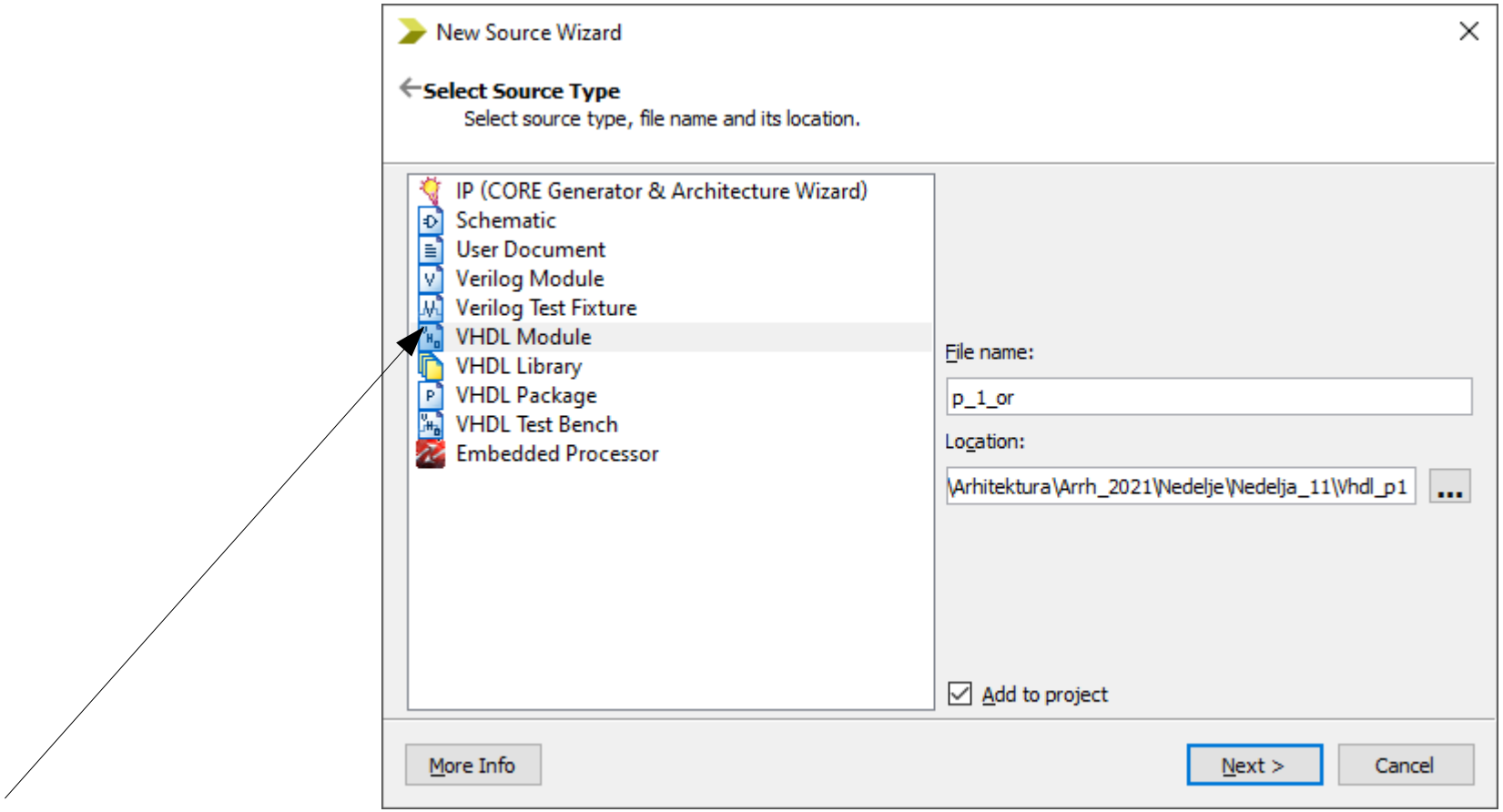
```
entity ili2 is

            port ( A, B   : in        BIT;
                   Z      :     out   BIT );
end ili2;
```

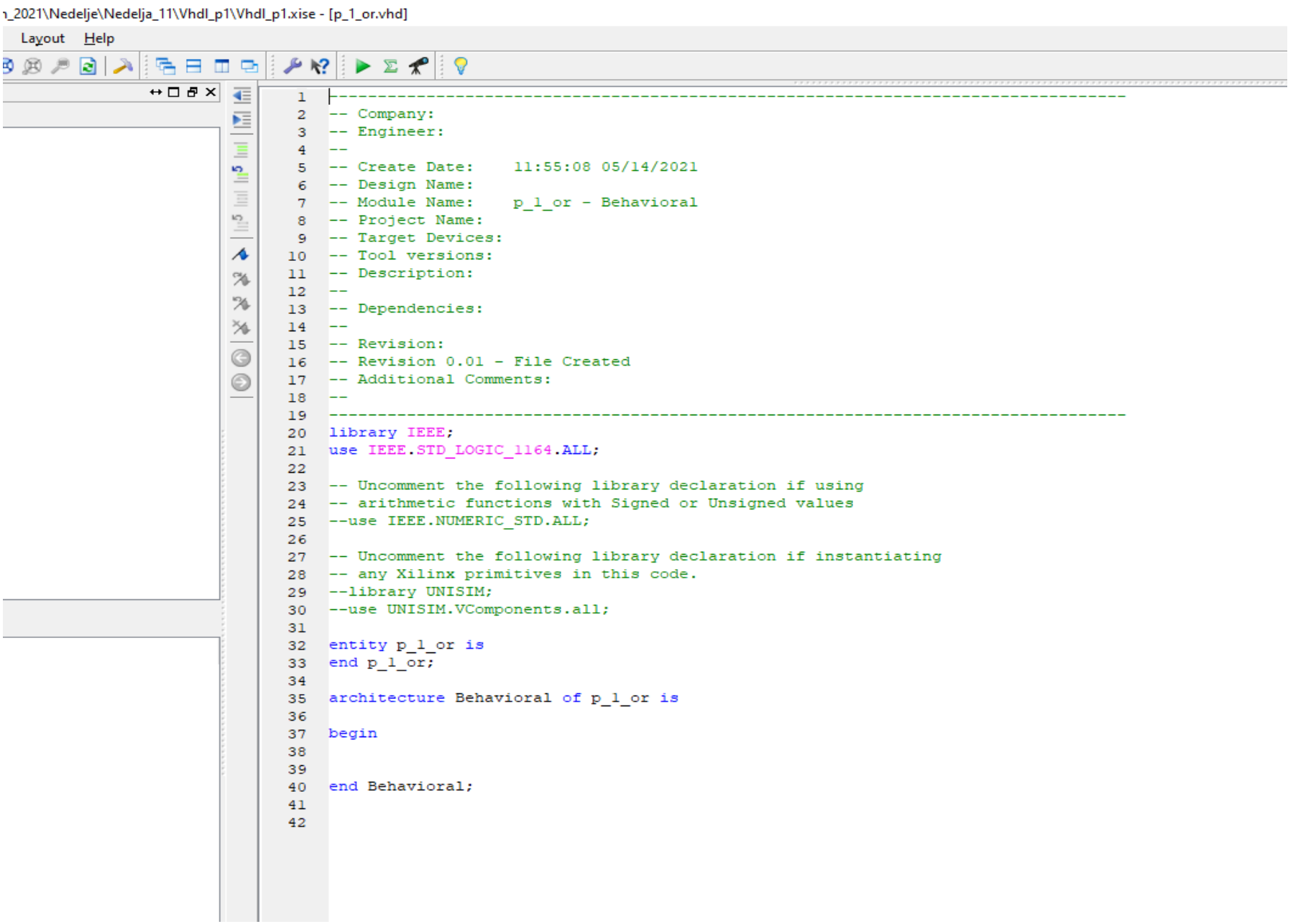

New Project Wizard
Create New Project
Specify project location and type.
Enter a name, locations, and comment for the project
Name: Vhdl_p1
Location: D:\fakultet\Pmf\Arhitektura\Arrh_2021\Nedelje\Nedelja_11\Vhdl_p1
Working Directory: D:\fakultet\Pmf\Arhitektura\Arrh_2021\Nedelje\Nedelja_11\Vhdl_p1
Description:
Select the type of top-level source for the project
Top-level source type:
HDL
More Info
Next >
Cancel


New Project Wizard
Project Settings
Specify device and project properties.
Select the device and design flow for the project
Property Name
Value
Evaluation Development Board
None Specified
Product Category
All
Family
Spartan3E
Device
XC3S1200E
Package
FG320
Speed
-5
Top-Level Source Type
HDL
Synthesis Tool
XST (VHDL/Verilog)
Simulator
ISim (VHDL/Verilog)
Preferred Language
Verilog
Property Specification in Project File
Store all values
Manual Compile Order
VHDL Source Analysis Standard
VHDL-93
Enable Message Filtering
More Info
< Back
Next >
Cancel


New Project Wizard
Project Summary
Project Navigator will create a new project with the following specifications.
Project:
Project Name: Vhdl_p1
Project Path: D:\fakultet\Pmf\Arhitektura\Arrh_2021\Nedelje\Nedelja_11\Vhdl_p1
Working Directory: D:\fakultet\Pmf\Arhitektura\Arrh_2021\Nedelje\Nedelja_11\Vhdl_p1
Description:
Top Level Source Type: HDL
Device:
Device Family: Spartan3E
Device: xc3s1200e
Package: fg320
Speed: -5
Top-Level Source Type: HDL
Synthesis Tool: XST (VHDL/Verilog)
Simulator: ISim (VHDL/Verilog)
Preferred Language: Verilog
Property Specification in Project File: Store all values
Manual Compile Order: false
VHDL Source Analysis Standard: VHDL-93
Message Filtering: disabled
More Info
< Back
Finish
Cancel


ISE Project Navigator (P.20131013) - D:\fakultet\Pmf\Arhitektura\Arrh_2021\Nedelje\Nedelja_11\Vhdl_p1\Vhdl_p1.xise
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
Vhdl_p1
xc3s1200e-5fg320
Empty View
The view currently contains no files. You can add files to the project using the toolbar at left, commands from the Project menu, and by using the Design, Files, and Libraries panels.
Use:
• New Source: To create a new source file.
• Add Source: To add an existing file to the project.
• Add Copy of Source: To copy an existing file to the project directory and add it to the project.
No Processes Running
No single design module is selected.
Design Utilities
Start Design Files Libraries


New Source Wizard
Select Source Type
Select source type, file name and its location.
IP (CORE Generator & Architecture Wizard)
Schematic
User Document
Verilog Module
Verilog Test Fixture
VHDL Module
VHDL Library
VHDL Package
VHDL Test Bench
Embedded Processor
File name:
p_1_or
Location:
\Arhitektura\Arrh_2021\Nedelje\Nedelja_11\Vhdl_p1
...
Add to project
More Info
Next >
Cancel

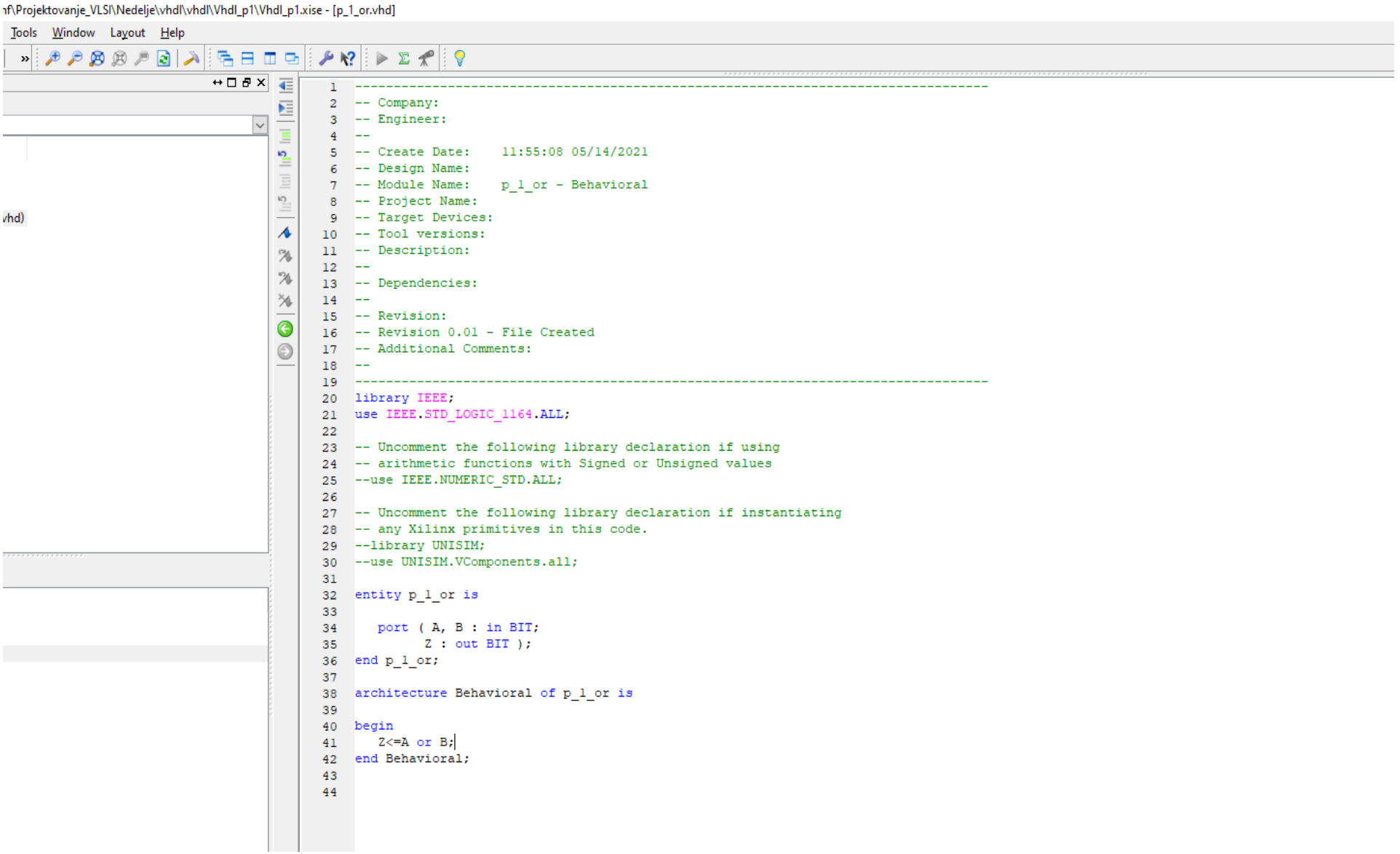

_2021\Nedelje\Nedelja_11\Vhdl_p1\Vhdl_p1.xise - [p_1_or.vhd]
Layout
Help
1 ----------
2 -- Company:
3 -- Engineer:
4 --
5 -- Create Date: 11:55:08 05/14/2021
6 -- Design Name:
7 -- Module Name: p_1_or - Behavioral
8 -- Project Name:
9 -- Target Devices:
10 -- Tool versions:
11 -- Description:
12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19 ----------
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22
23 -- Uncomment the following library declaration if using
24 -- arithmetic functions with Signed or Unsigned values
25 --use IEEE.NUMERIC_STD.ALL;
26
27 -- Uncomment the following library declaration if instantiating
28 -- any Xilinx primitives in this code.
29 --library UNISIM;
30 --use UNISIM.VComponents.all;
31
32 entity p_1_or is
33 end p_1_or;
34
35 architecture Behavioral of p_1_or is
36
37 begin
38
39
40 end Behavioral;
41
42

nf\Arhitektura\Arrh_2021\Nedelje\Nedelja_11\Vhdl_p1\Vhdl_p1.xise - [p_1_or.vhd]

Tools Window Layout Help

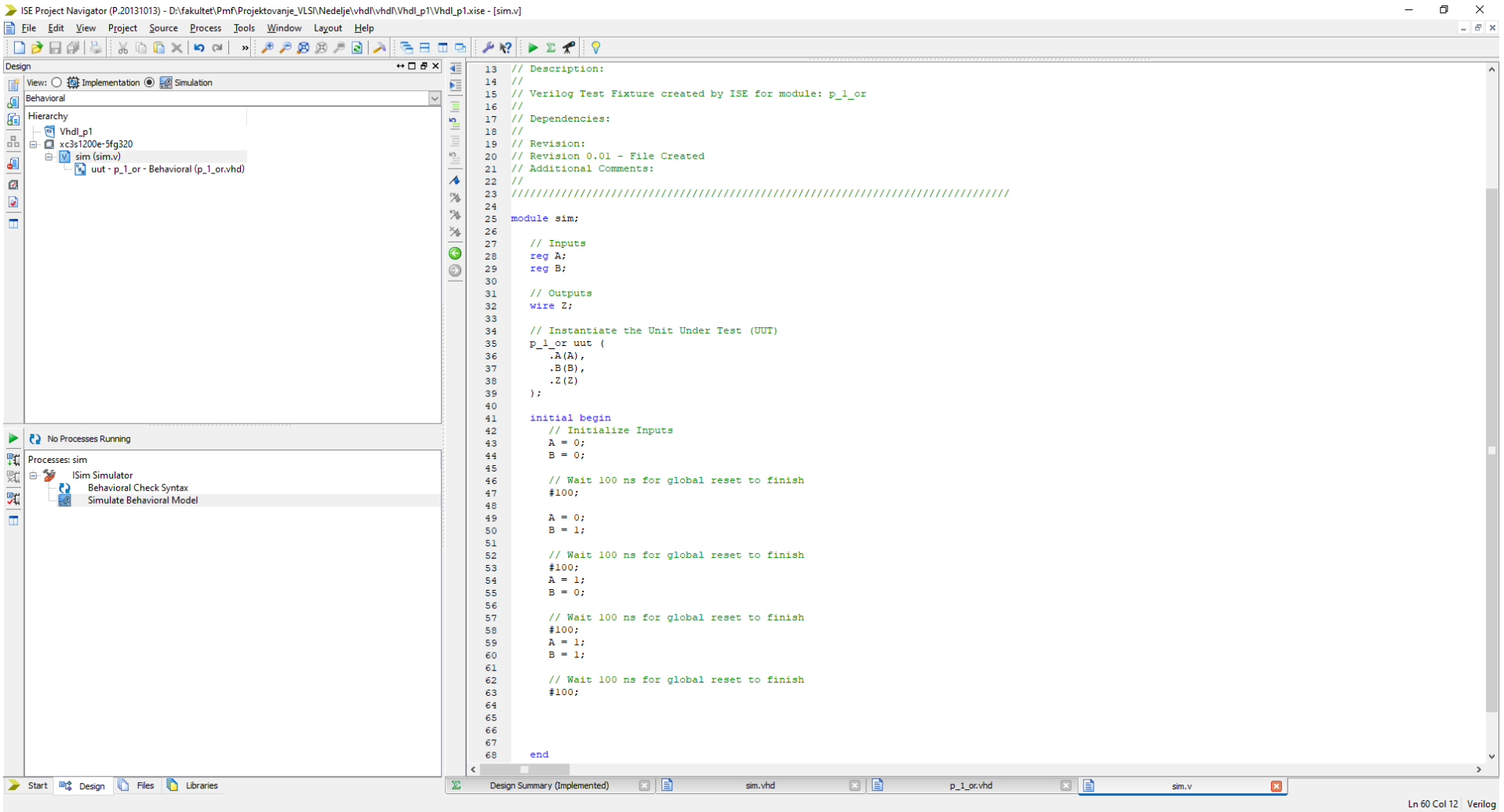
```
1  ----------------------------------------------------------------------------------
2  -- Company:
3  -- Engineer:
4  --
5  -- Create Date:    11:55:08 05/14/2021
6  -- Design Name:
7  -- Module Name:    p_1_or - Behavioral
8  -- Project Name:
9  -- Target Devices:
10 -- Tool versions:
11 -- Description:
12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19 ----------------------------------------------------------------------------------
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22
23 -- Uncomment the following library declaration if using
24 -- arithmetic functions with Signed or Unsigned values
25 --use IEEE.NUMERIC_STD.ALL;
26
27 -- Uncomment the following library declaration if instantiating
28 -- any Xilinx primitives in this code.
29 --library UNISIM;
30 --use UNISIM.VComponents.all;
31
32 entity p_1_or is
33
34    port ( A, B : in BIT;
35           Z : out BIT );
36 end p_1_or;
37
38 architecture Behavioral of p_1_or is
39
40 begin
41
42
43 end Behavioral;
44
45
```

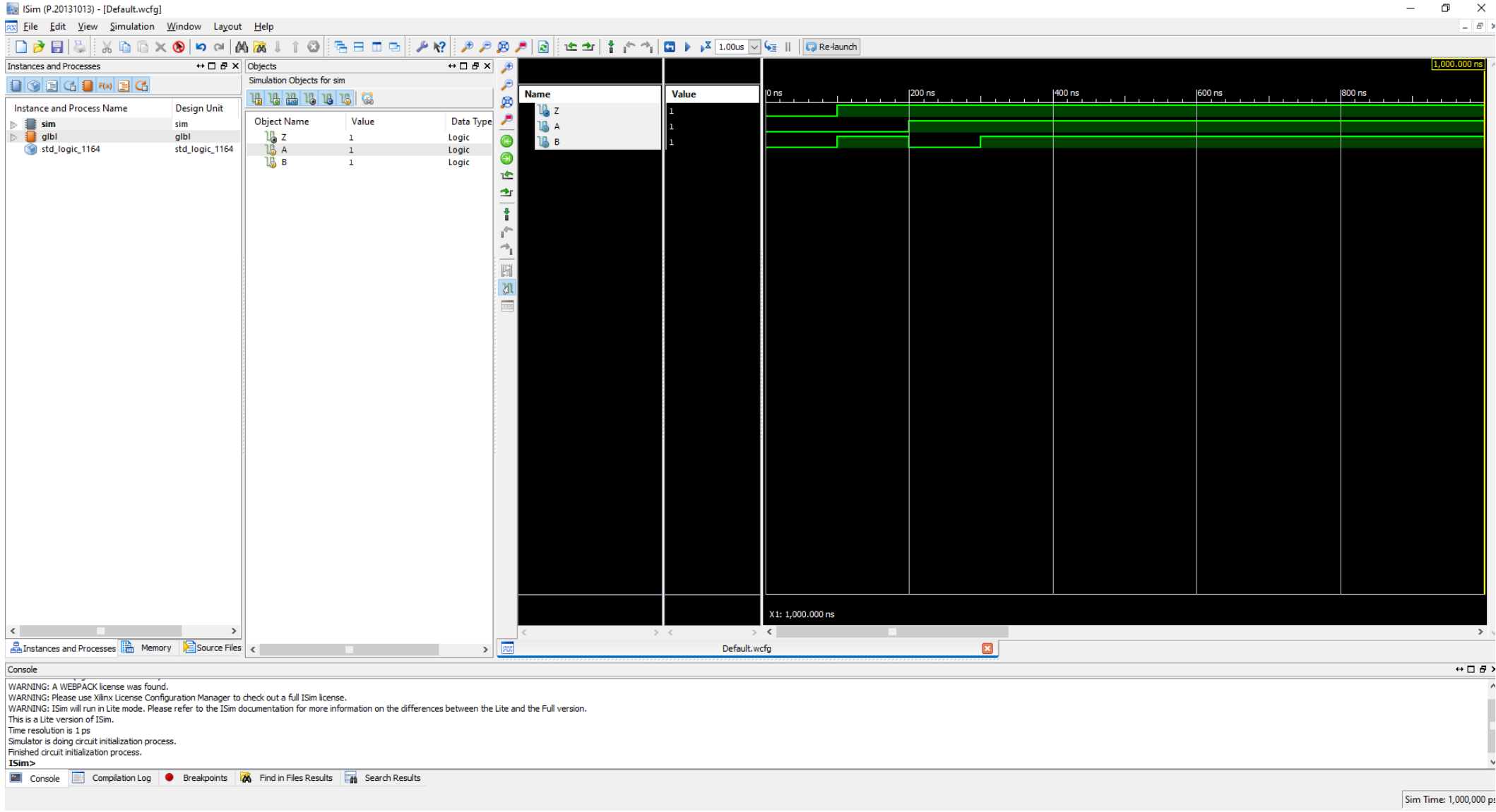
Za logičko ILI definisati arhitekturu koja će obavljati logičku ili funkciju Z= A+B




```
1  ----------------------------------------------------------------------------------
2  -- Company:
3  -- Engineer:
4  --
5  -- Create Date:    11:55:08 05/14/2021
6  -- Design Name:
7  -- Module Name:    p_1_or - Behavioral
8  -- Project Name:
9  -- Target Devices:
10 -- Tool versions:
11 -- Description:
12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19 ----------------------------------------------------------------------------------
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22
23 -- Uncomment the following library declaration if using
24 -- arithmetic functions with Signed or Unsigned values
25 --use IEEE.NUMERIC_STD.ALL;
26
27 -- Uncomment the following library declaration if instantiating
28 -- any Xilinx primitives in this code.
29 --library UNISIM;
30 --use UNISIM.VComponents.all;
31
32 entity p_1_or is
33
34    port ( A, B : in BIT;
35           Z : out BIT );
36 end p_1_or;
37
38 architecture Behavioral of p_1_or is
39
40 begin
41    Z<=A or B;
42 end Behavioral;
43
44
```

Moze da se koristi isti Verilog Test Sim




ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instances and Processes
Instance and Process Name
Design Unit
sim
glbl
std_logic_1164
Objects
Simulation Objects for sim
Object Name
Value
Data Type
Z 1 Logic
A 1 Logic
B 1 Logic
Name
Value
1,000.000 ns
0 ns
200 ns
400 ns
600 ns
800 ns
X1: 1,000.000 ns
Instances and Processes
Memory
Source Files
Default.wcfg
Console
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps