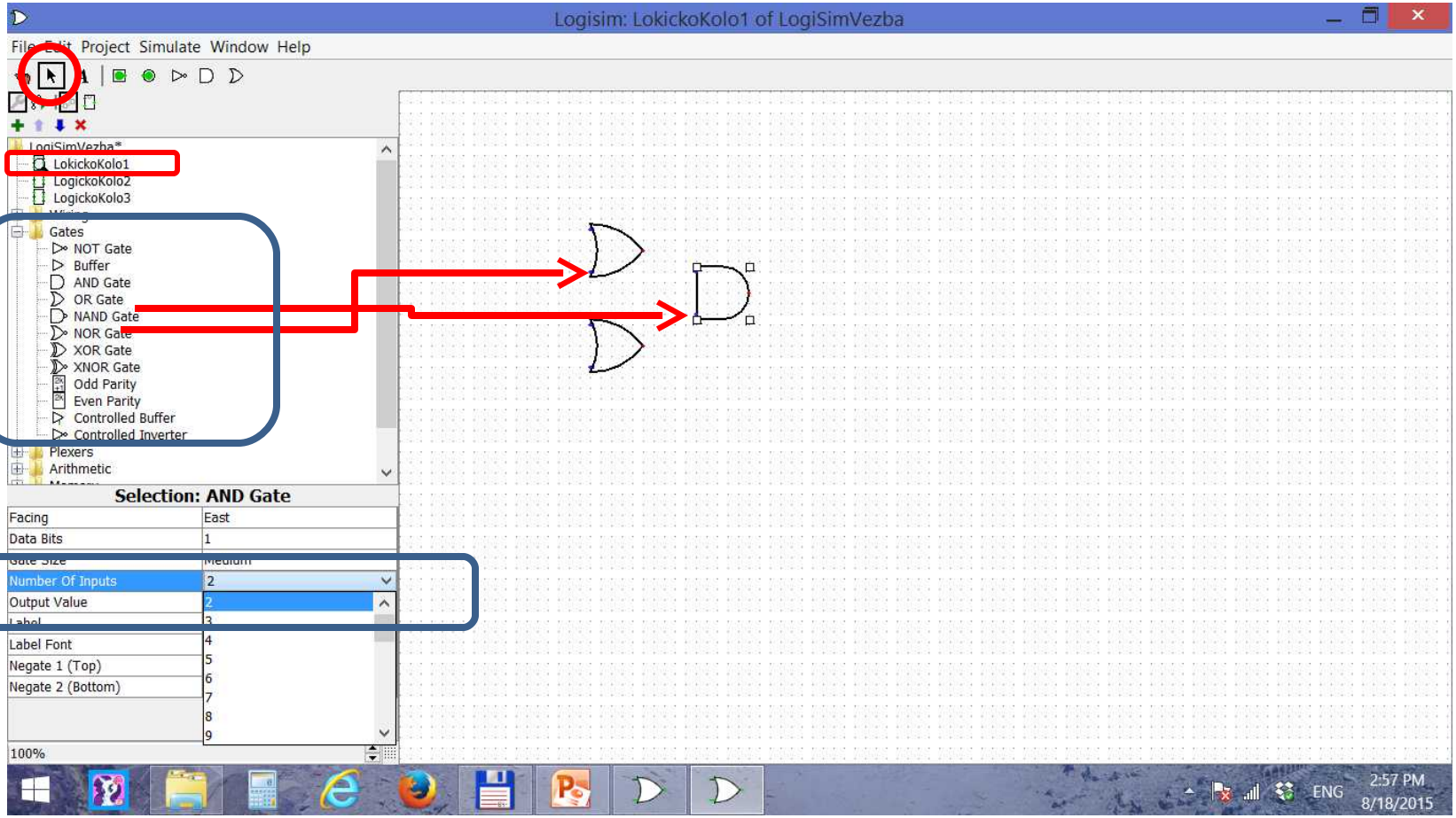
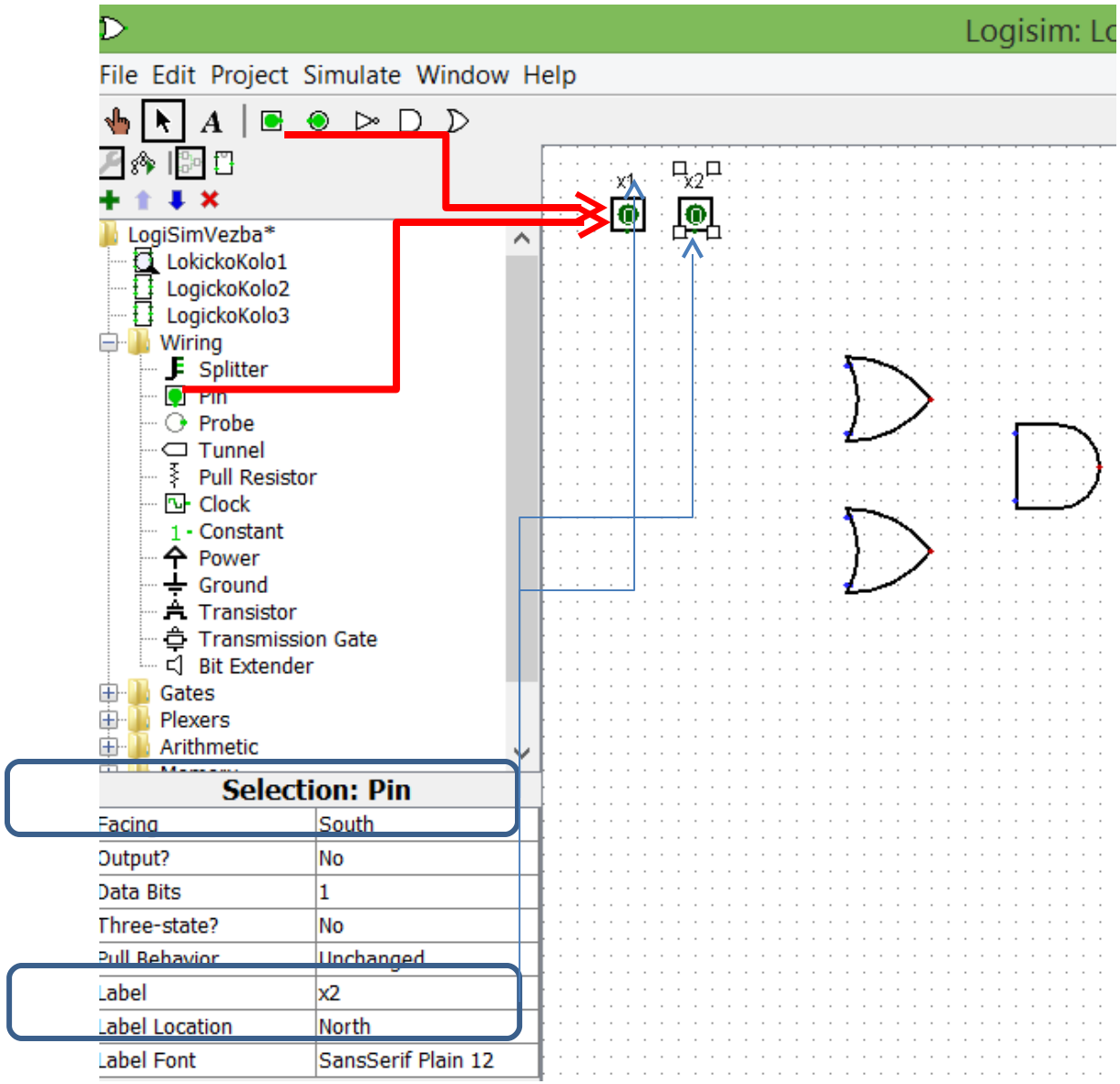
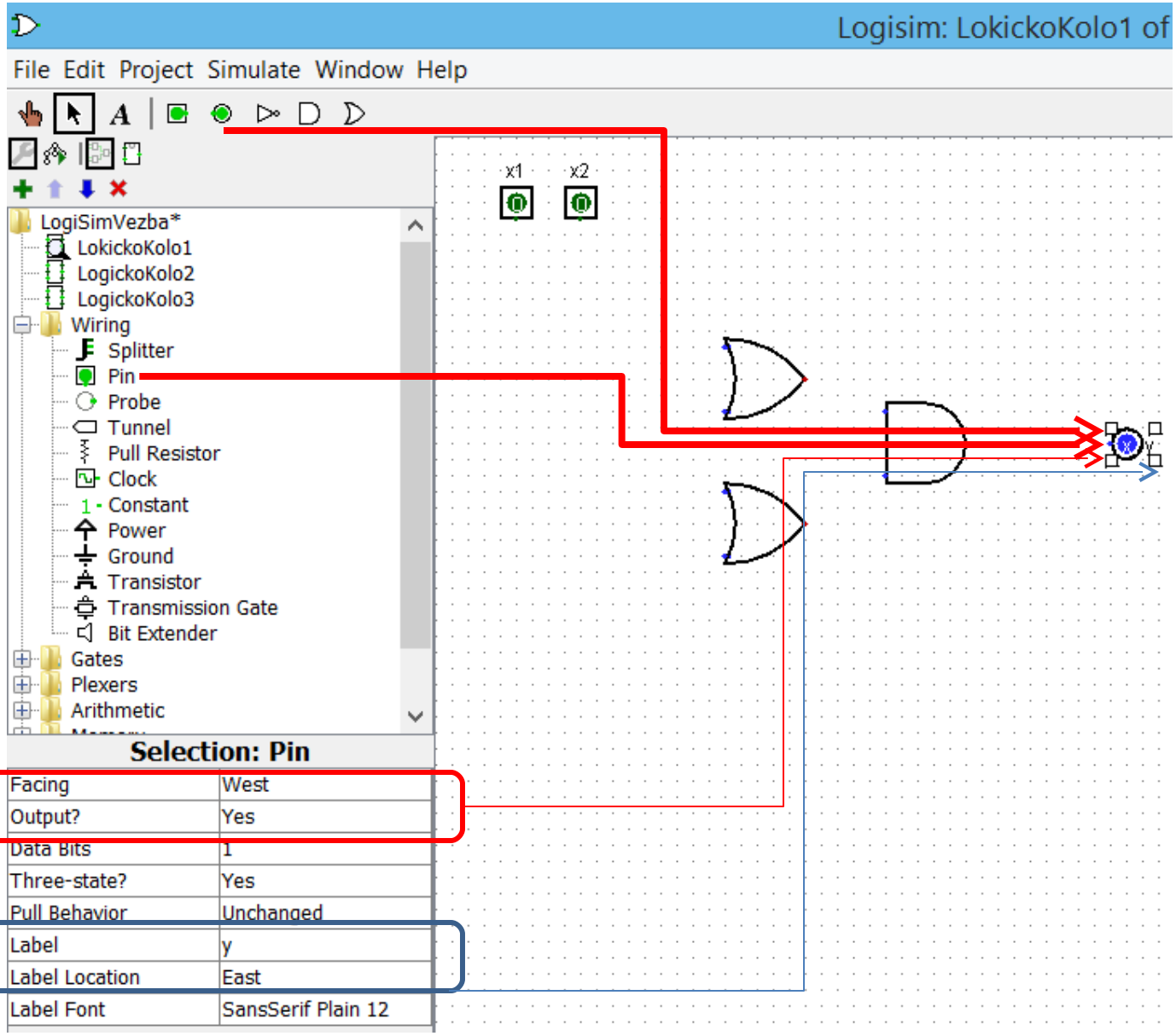
LogiSim

LogiSim

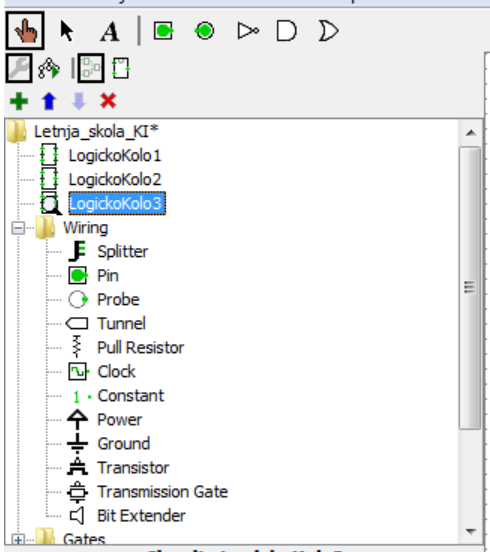

Logisim: LokickoKolo1 of LogiSimVezba
File Edit Project Simulate Window Help
LogiSimVezba*
LokickoKolo1
LogickoKolo2
LogickoKolo3
Gates
NOT Gate
Buffer
AND Gate
OR Gate
NAND Gate
NOR Gate
XOR Gate
XNOR Gate
Odd Parity
Even Parity
Controlled Buffer
Controlled Inverter
Plexers
Arithmetic
Selection: AND Gate
Facing
East
Data Bits
1
Number Of Inputs
2
Output Value
Label Font
Negate 1 (Top)
Negate 2 (Bottom)
2
3
4
5
6
7
8
9
100%
ENG
2:57 PM
8/18/2015


Logisim: Lo
File Edit Project Simulate Window Help
LogiSimVezba*
LokickoKolo1
LogickoKolo2
LogickoKolo3
Wiring
Splitter
Pin
Probe
Tunnel
Pull Resistor
Clock
Constant
Power
Ground
Transistor
Transmission Gate
Bit Extender
Gates
Plexers
Arithmetic
x1
x2
Selection: Pin
Facing South
Output? No
Data Bits 1
Three-state? No
Pull Behavior Unchanged
Label x2
Label Location North
Label Font SansSerif Plain 12


Logisim: LokickoKolo1 of
File Edit Project Simulate Window Help
LogiSimVezba*
LokickoKolo1
LogickoKolo2
LogickoKolo3
Wiring
Splitter
Pin
Probe
Tunnel
Pull Resistor
Clock
Constant
Power
Ground
Transistor
Transmission Gate
Bit Extender
Gates
Plexers
Arithmetic
Selection: Pin
Facing West
Output? Yes
Data Bits 1
Three-state? Yes
Pull Behavior Unchanged
Label y
Label Location East
Label Font SansSerif Plain 12
x1
x2
y

Logisim: LogickoKolo3 of Letnja_skola_KI

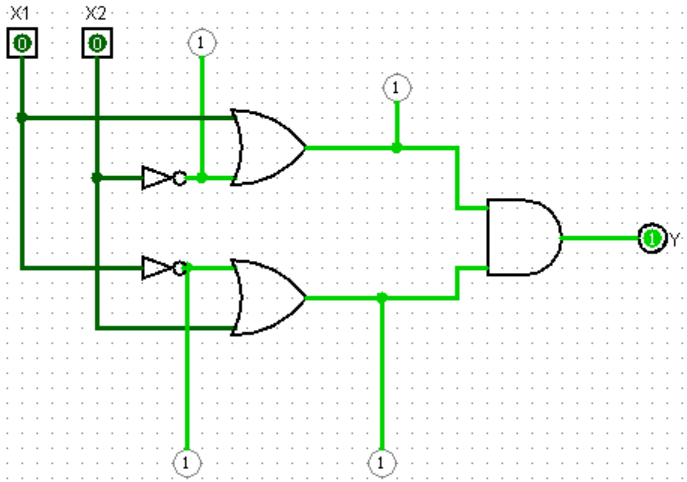
File Edit Project Simulate Window Help

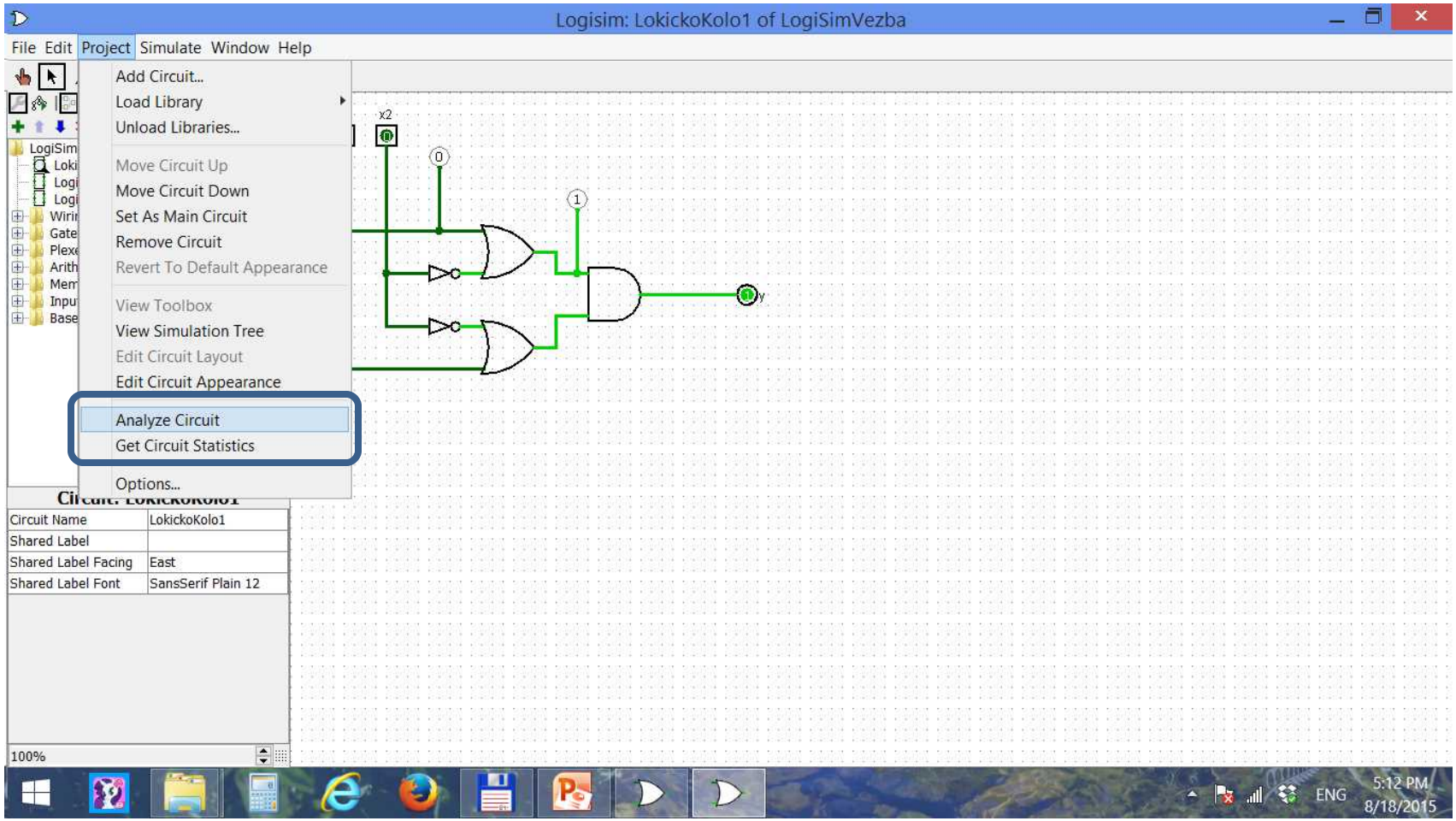


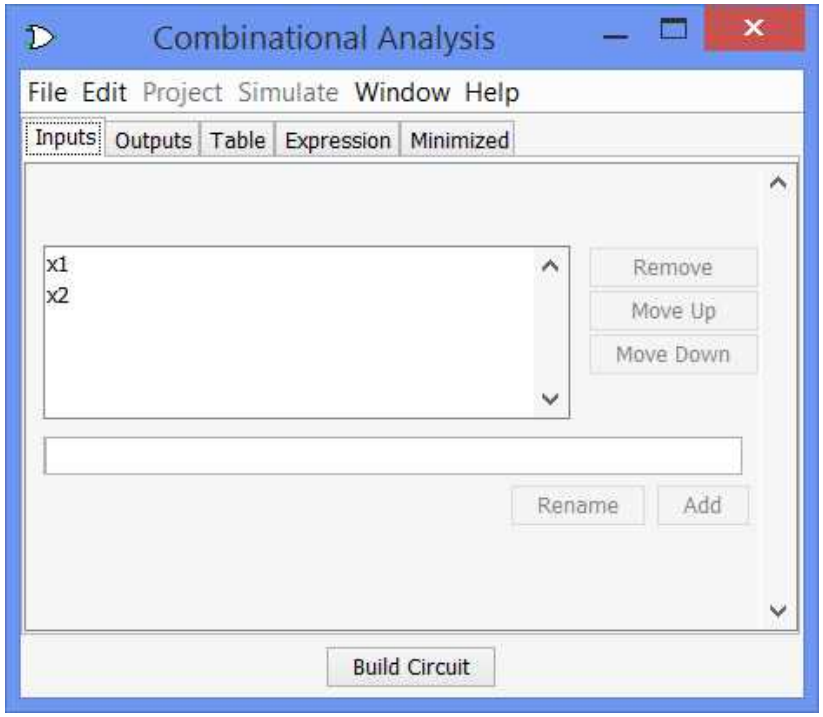
Circuit: LogickoKolo3

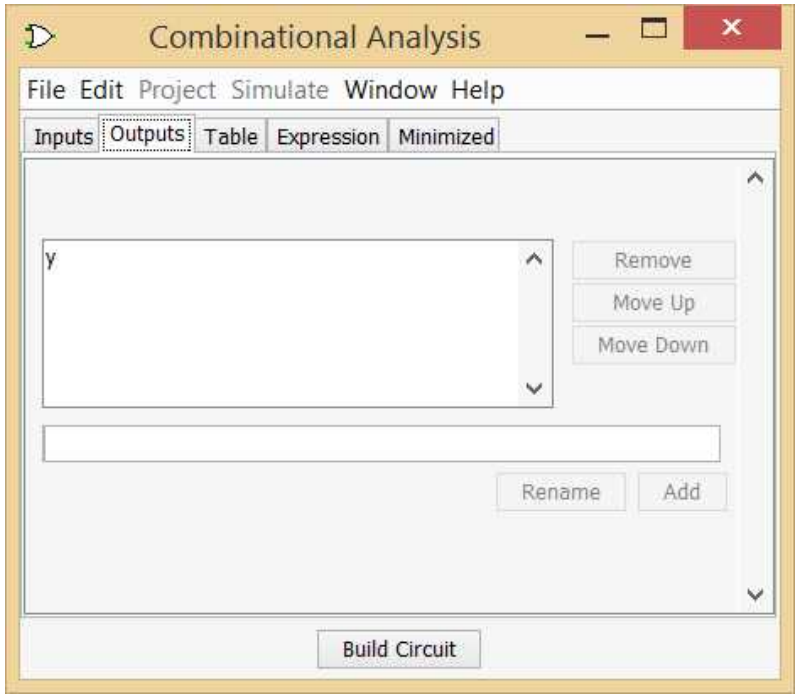
Circuit Name	LogickoKolo3
Shared Label	
Shared Label Facing	East
Shared Label Font	SansSerif Plain 12

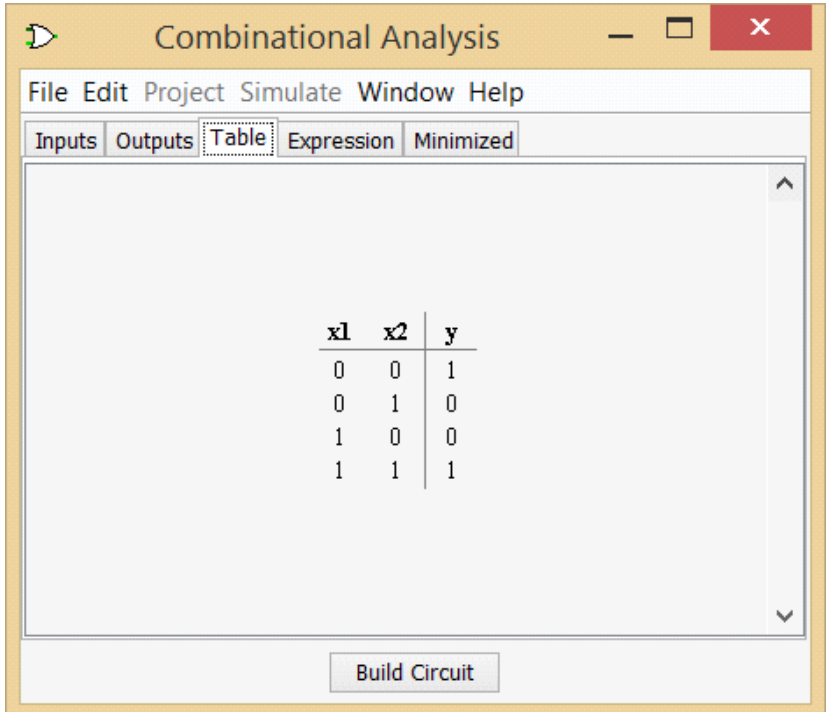
100%

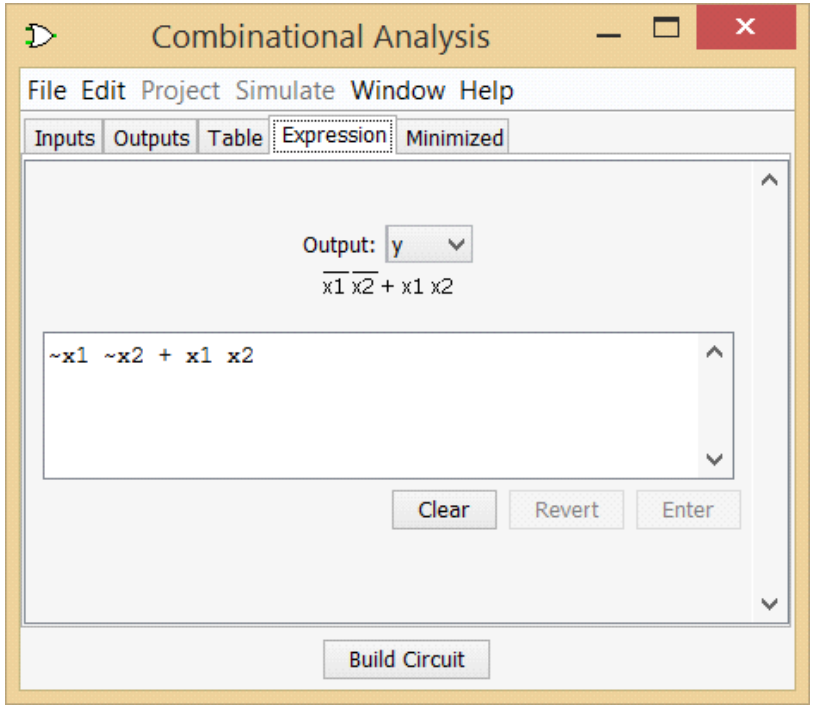


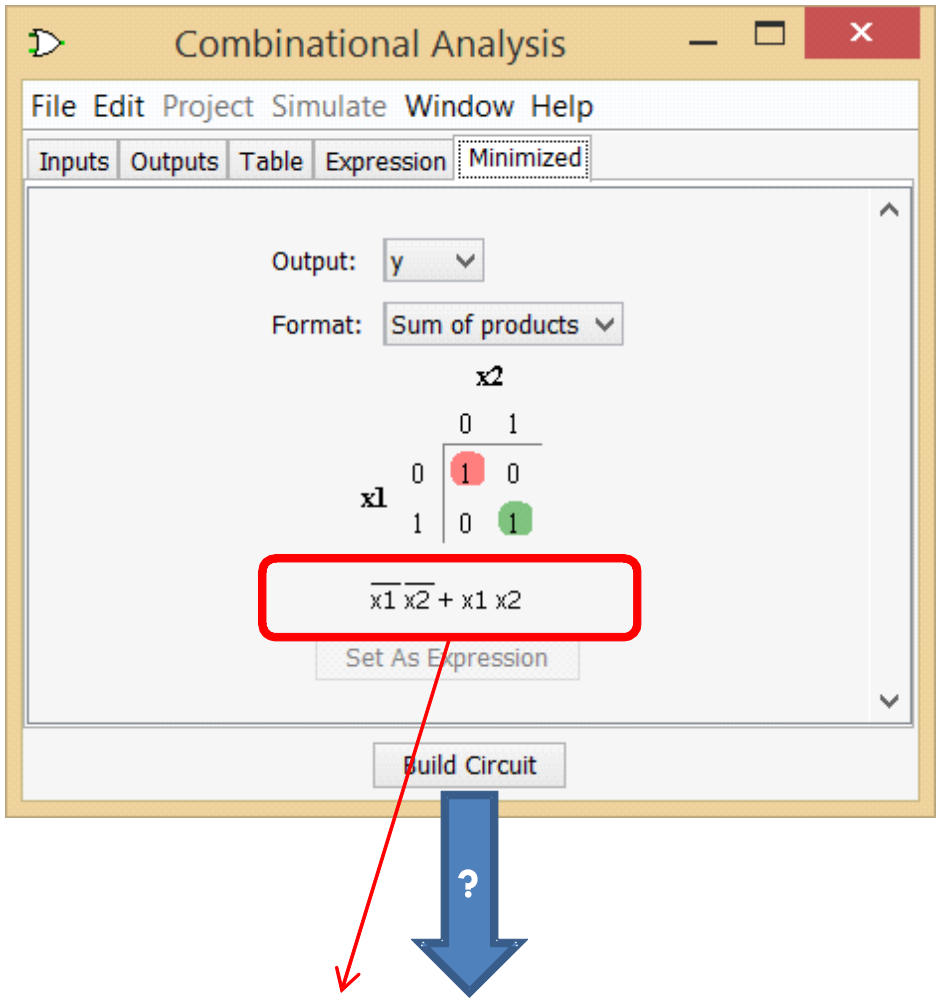

Logisim: LokickoKolo1 of LogiSimVezba
File Edit Project Simulate Window Help
Add Circuit...
Load Library
Unload Libraries...
Move Circuit Up
Move Circuit Down
Set As Main Circuit
Remove Circuit
Revert To Default Appearance
View Toolbox
View Simulation Tree
Edit Circuit Layout
Edit Circuit Appearance
Analyze Circuit
Get Circuit Statistics
Options...
x2
0
1
y
Circuit Name
LokickoKolo1
Shared Label
Shared Label Facing
East
Shared Label Font
SansSerif Plain 12
100%
ENG
5:12 PM
8/18/2015


Combinational Analysis
File Edit Project Simulate Window Help
Inputs Outputs Table Expression Minimized
x1
x2
Remove
Move Up
Move Down
Rename
Add
Build Circuit

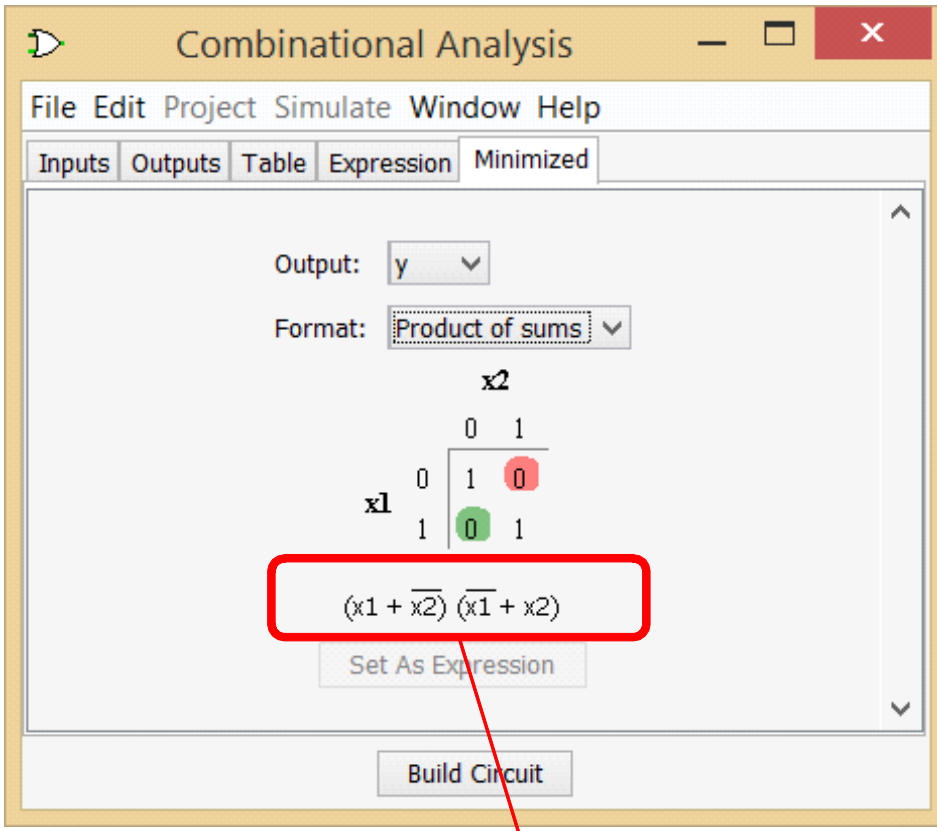

Combinational Analysis
File Edit Project Simulate Window Help
Inputs Outputs Table Expression Minimized
y
Remove
Move Up
Move Down
Rename
Add
Build Circuit


Combinational Analysis
File Edit Project Simulate Window Help
Inputs Outputs Table Expression Minimized
x1 x2 y
0 0 1
0 1 0
1 0 0
1 1 1
Build Circuit

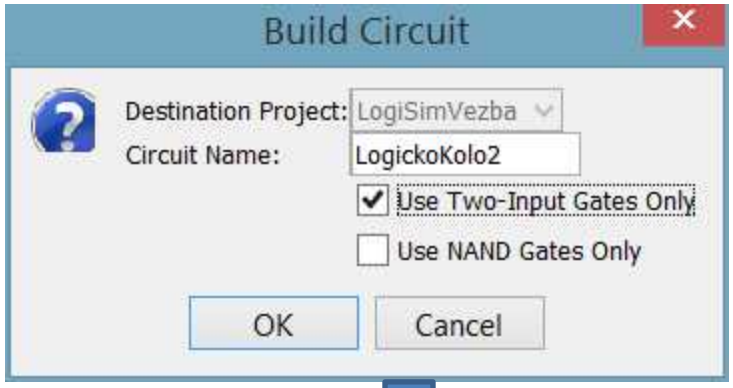

Combinational Analysis
File Edit Project Simulate Window Help
Inputs Outputs Table Expression Minimized
Output: y
x1 x2 + x1 x2
~x1 ~x2 + x1 x2
Clear
Revert
Enter
Build Circuit

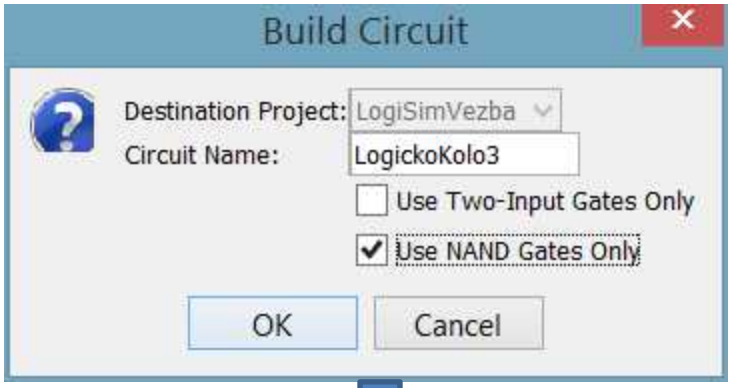


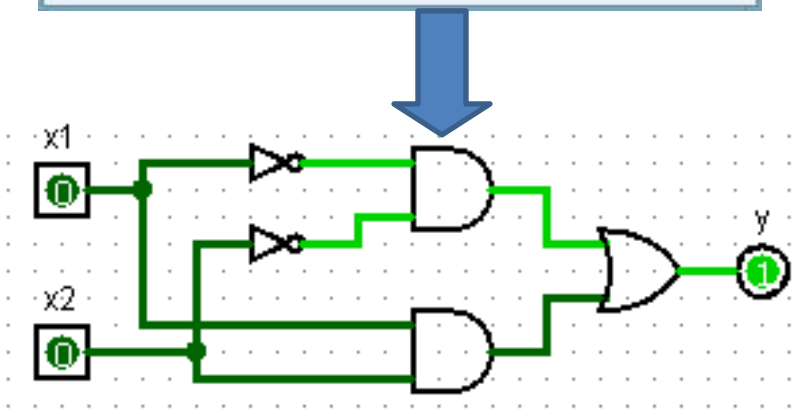
fminDNF

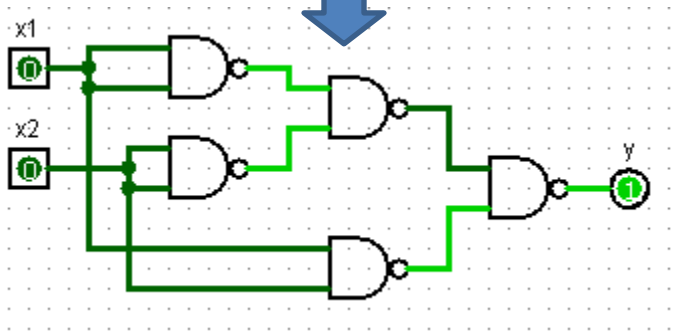


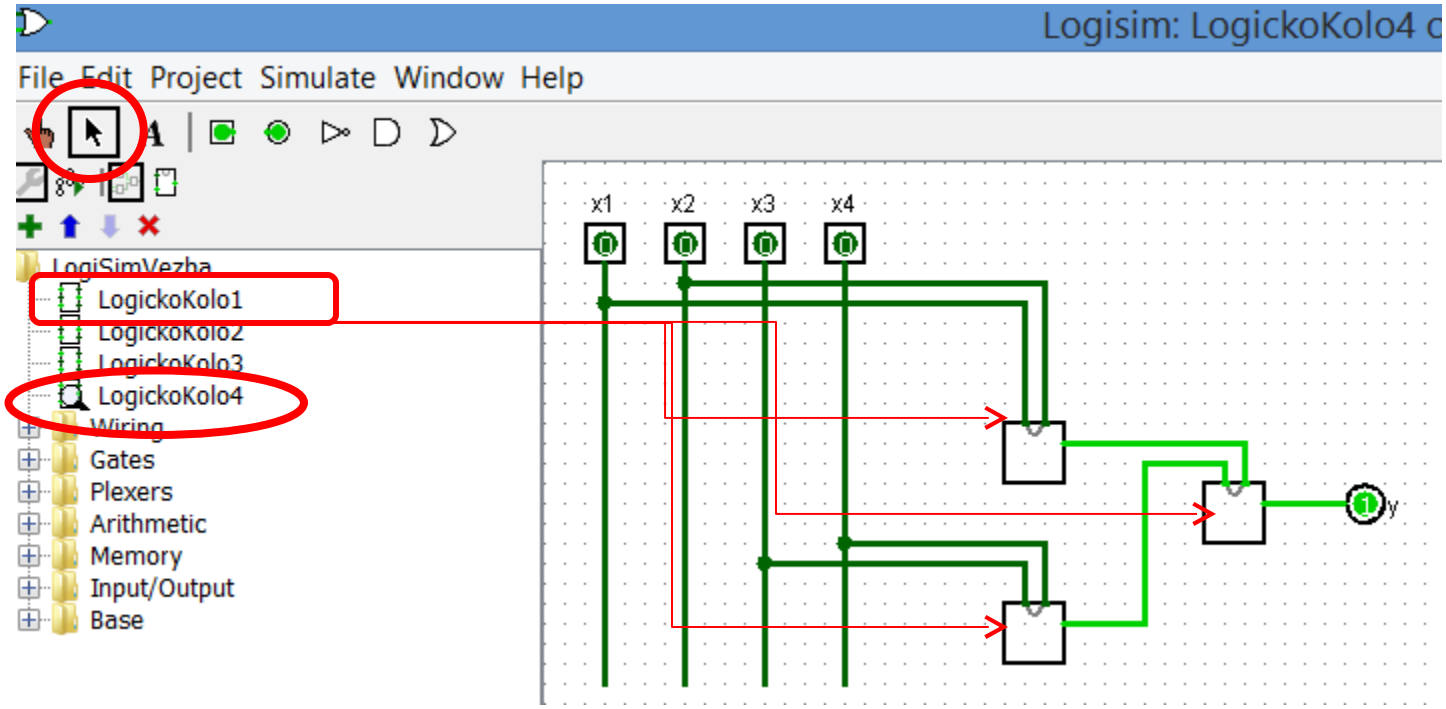
fminKNF

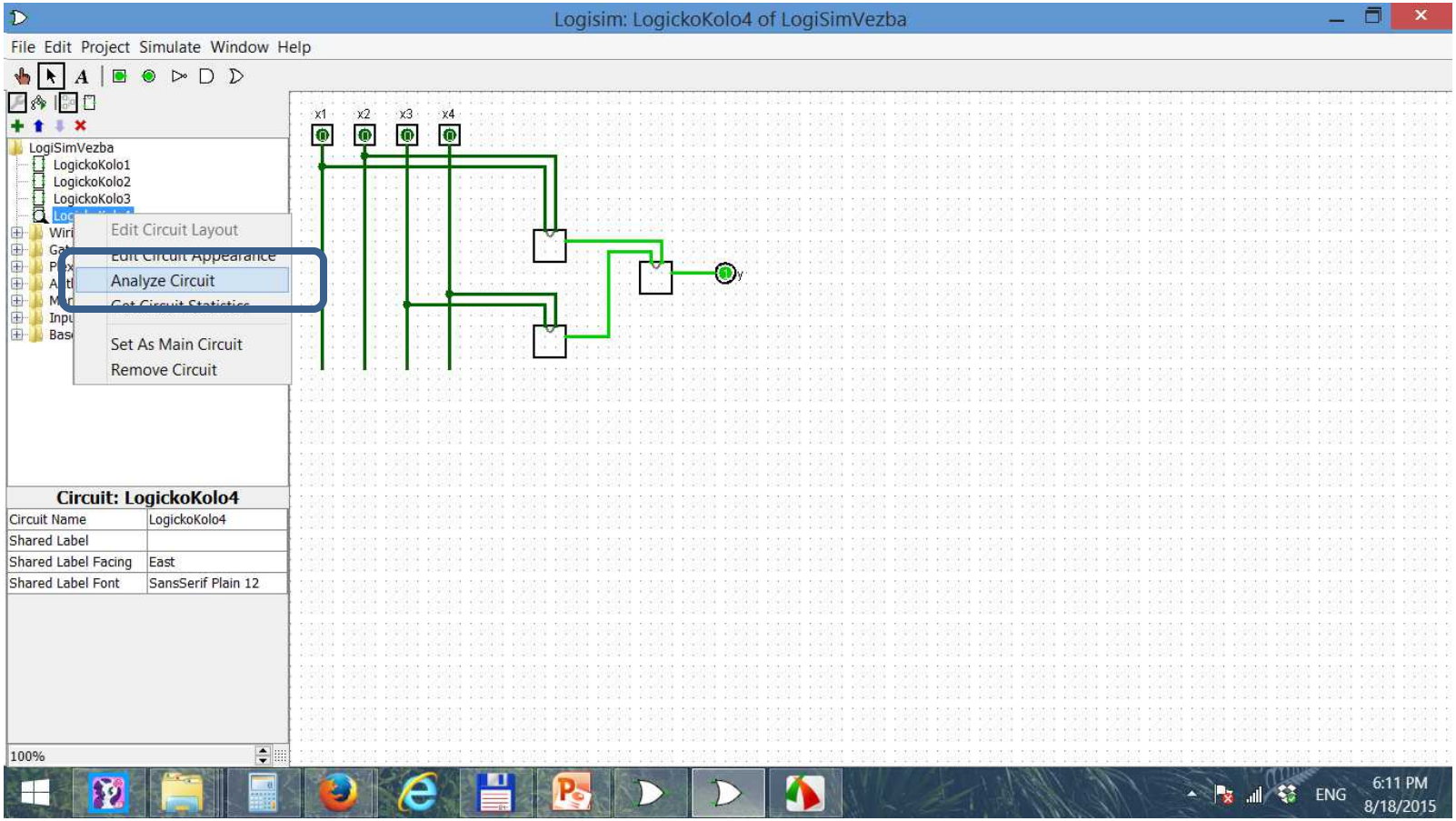

Build Circuit
Destination Project:
LogiSimVezba
Circuit Name:
LogickoKolo2
Use Two-Input Gates Only
Use NAND Gates Only
OK
Cancel

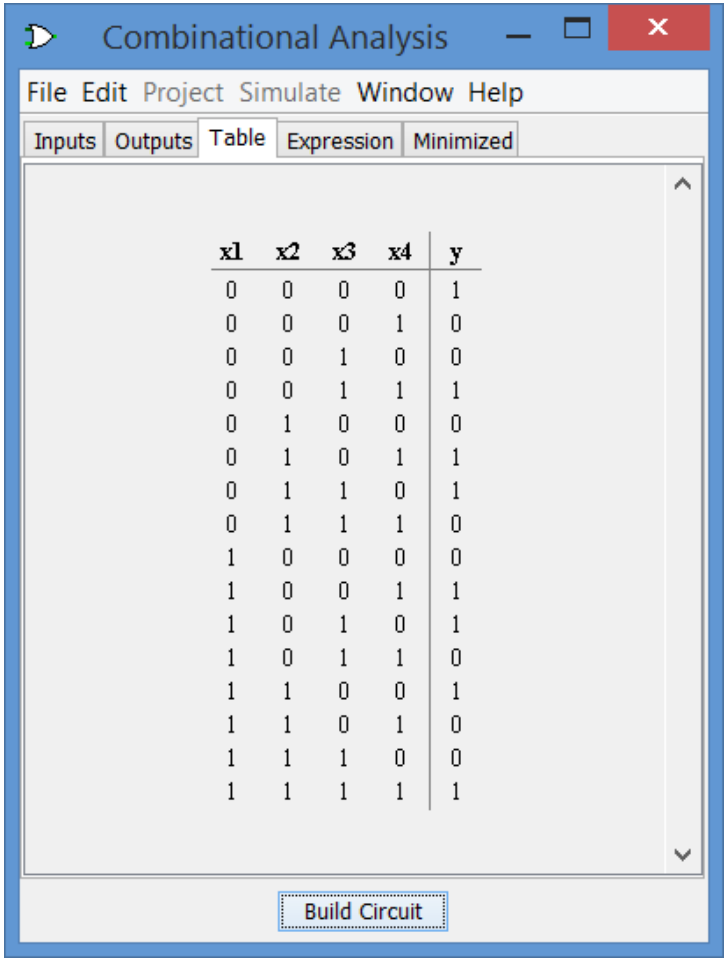

Build Circuit
Destination Project:
LogiSimVezba
Circuit Name:
LogickoKolo3
Use Two-Input Gates Only
Use NAND Gates Only
OK
Cancel

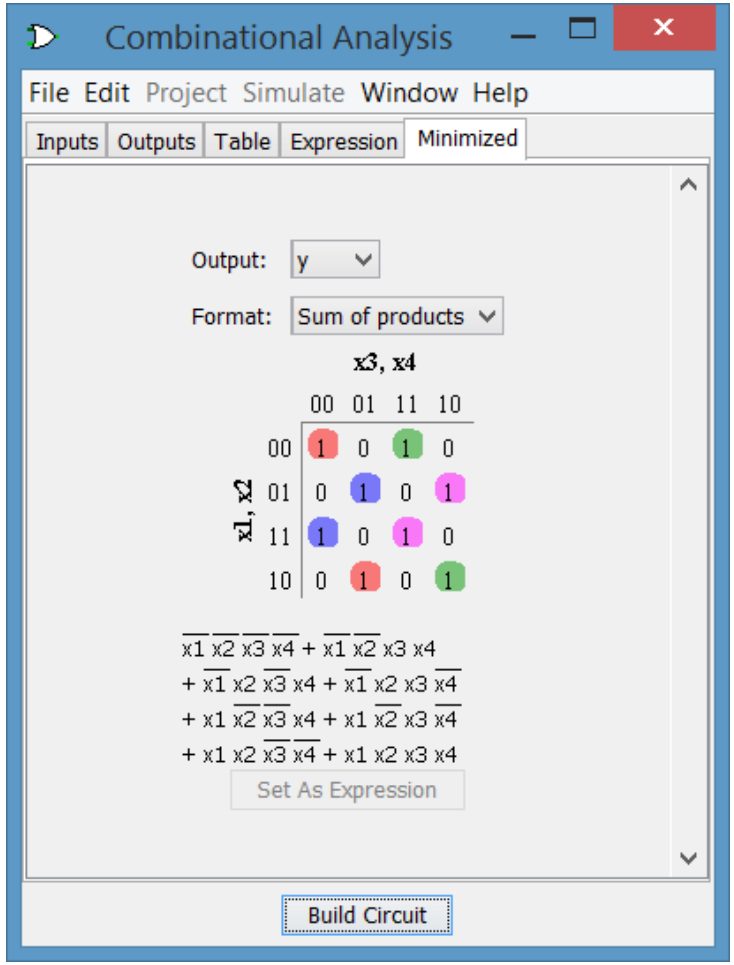

x1
x2
y


x1
x2
y

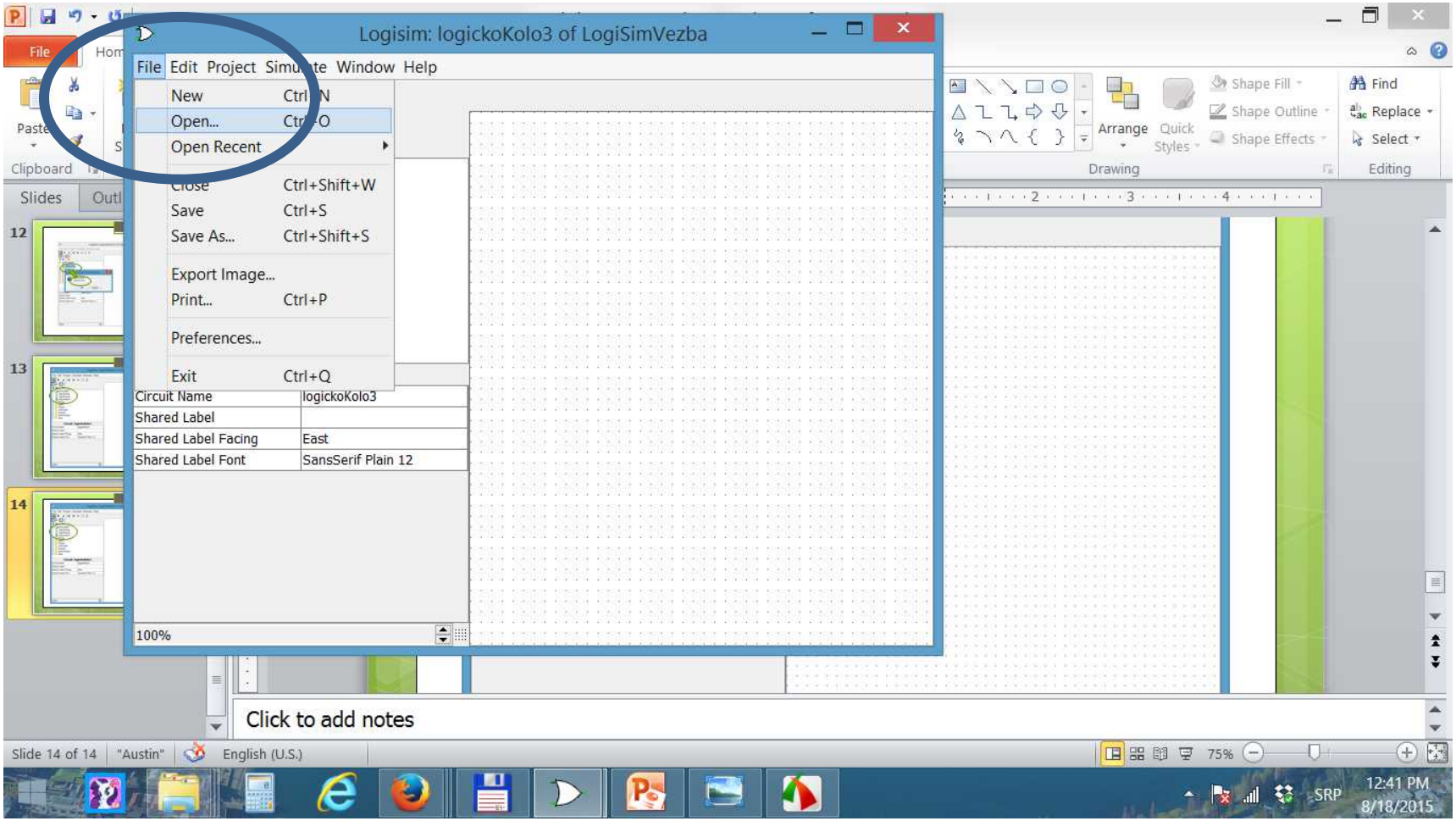

Logisim: LogickoKolo4 c
File Edit Project Simulate Window Help
LogiSimVezba
LogickoKolo1
LogickoKolo2
LogickoKolo3
LogickoKolo4
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
x1
x2
x3
x4
y


Logisim: LogickoKolo4 of LogiSimVezba
File Edit Project Simulate Window Help
LogiSimVezba
LogickoKolo1
LogickoKolo2
LogickoKolo3
Edit Circuit Layout
Analyze Circuit
Set As Main Circuit
Remove Circuit
x1
x2
x3
x4
y
Circuit: LogickoKolo4
Circuit Name
LogickoKolo4
Shared Label
Shared Label Facing
East
Shared Label Font
SansSerif Plain 12
100%
ENG
6:11 PM
8/18/2015


Combinational Analysis
File Edit Project Simulate Window Help
Inputs Outputs Table Expression Minimized
x1 x2 x3 x4 y
0 0 0 0 1
0 0 0 1 0
0 0 1 0 0
0 0 1 1 1
0 1 0 0 0
0 1 0 1 1
0 1 1 0 1
0 1 1 1 0
1 0 0 0 0
1 0 0 1 1
1 0 1 0 1
1 0 1 1 0
1 1 0 0 1
1 1 0 1 0
1 1 1 0 0
1 1 1 1 1
Build Circuit

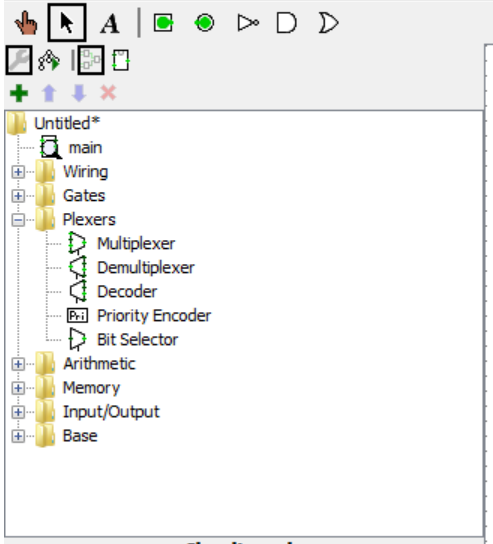

Combinational Analysis
File Edit Project Simulate Window Help
Inputs Outputs Table Expression Minimized
Output: y
Format: Sum of products
x3, x4
00 01 11 10
x1, x2
00 1 0 1 0
01 0 1 0 1
11 1 0 1 0
10 0 1 0 1
x1 x2 x3 x4 + x1 x2 x3 x4
+ x1 x2 x3 x4 + x1 x2 x3 x4
+ x1 x2 x3 x4 + x1 x2 x3 x4
+ x1 x2 x3 x4 + x1 x2 x3 x4
Set As Expression
Build Circuit

Realizovati dekoder 3 - 8



Logisim: main of Untitled

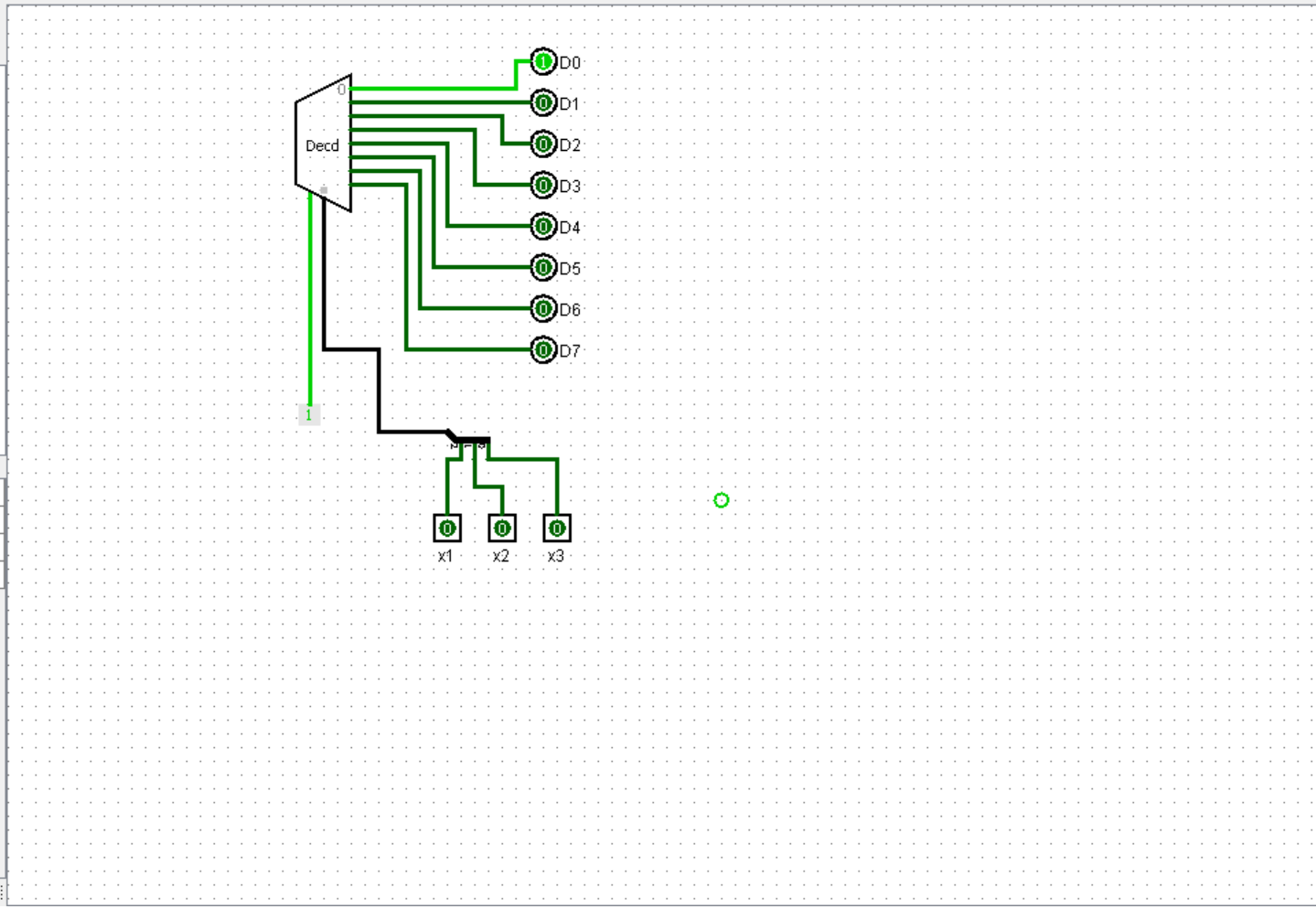
File Edit Project Simulate Window Help



Circuit: main

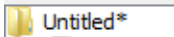
Circuit Name	main
Shared Label	
Shared Label Facing	East
Shared Label Font	SansSerif Plain 12

100%



Logisim: main of Untitled

File Edit Project Simulate Window Help

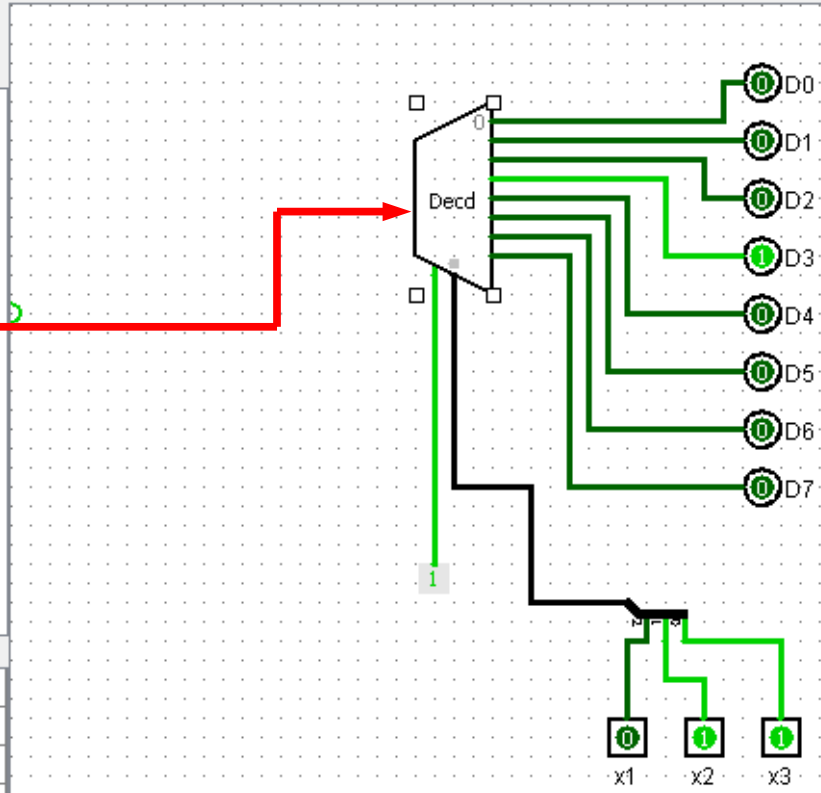


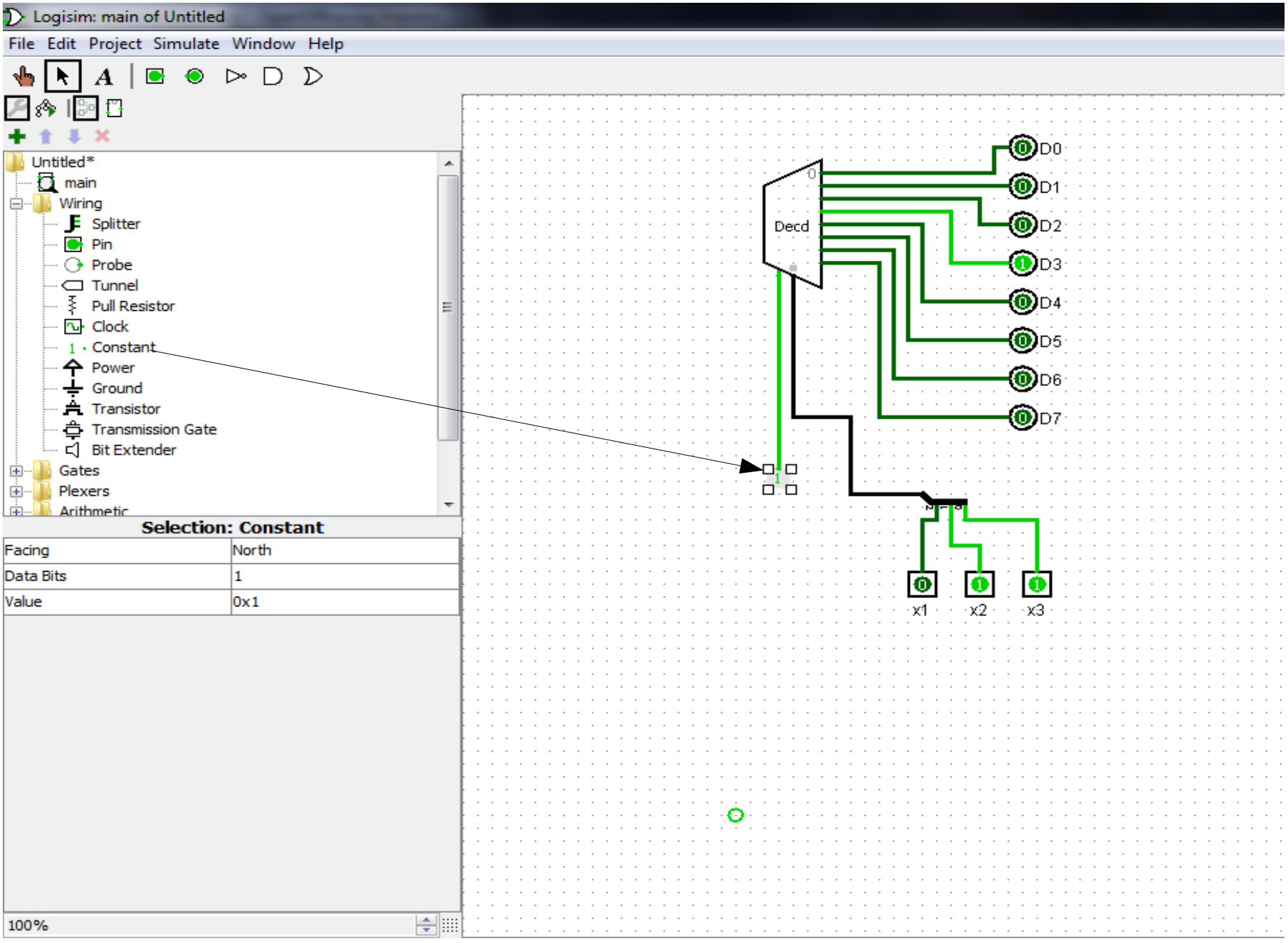
- Untitled*
  - main
  - Wiring
  - Gates
  - Plexers
    - Multiplexer
    - Demultiplexer
    - Decoder
    - Priority Encoder
    - Bit Selector
  - Arithmetic
  - Memory
  - Input/Output
  - Base

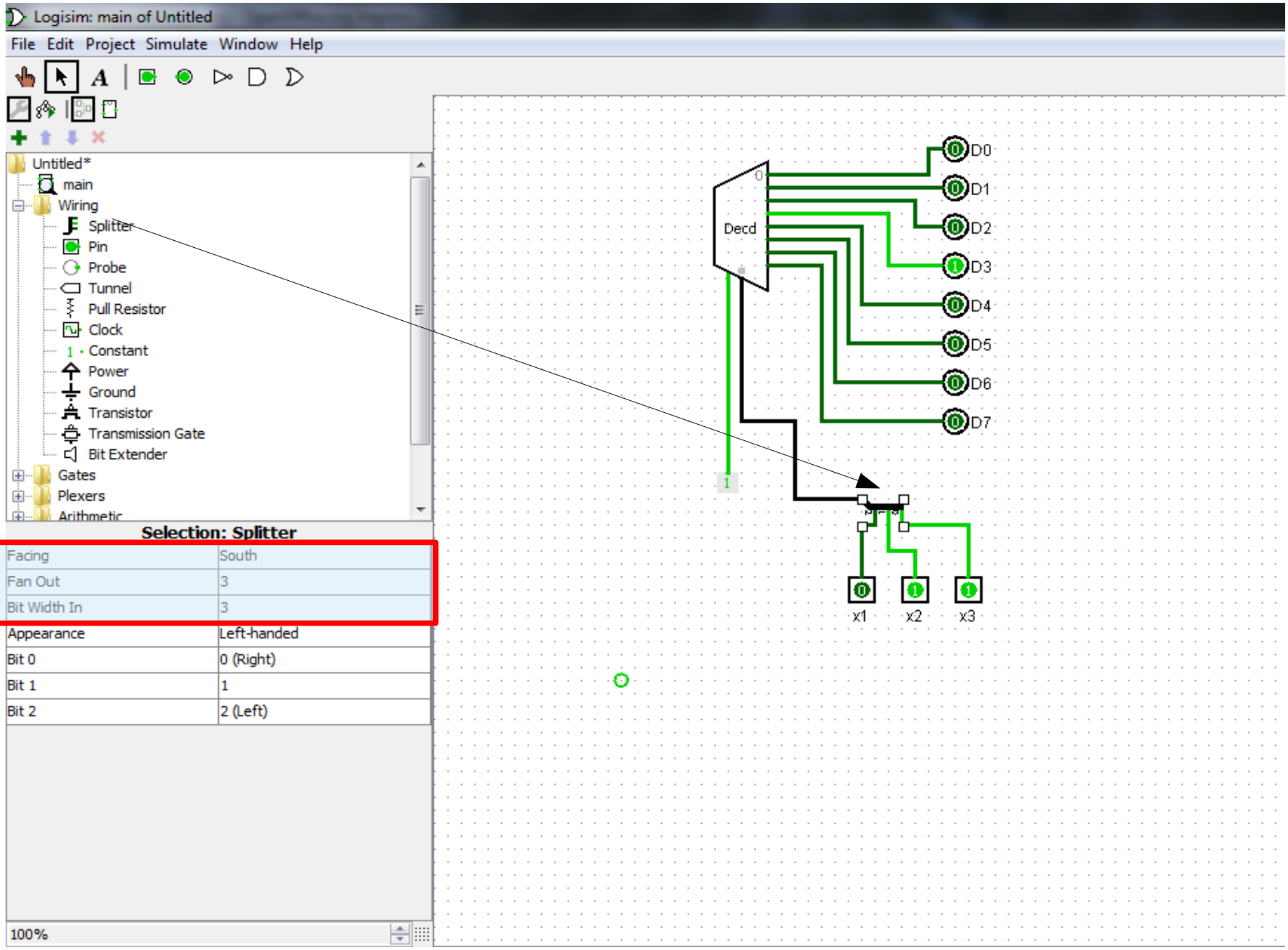
Selection: Decoder

Facing	East
Select Location	Bottom/Left
Select Bits	3
Three-state?	No
Disabled Output	Floating
Include Enable?	Yes

100%




Logisim: main of Untitled
File Edit Project Simulate Window Help
Untitled*
main
Wiring
Splitter
Pin
Probe
Tunnel
Pull Resistor
Clock
Constant
Power
Ground
Transistor
Transmission Gate
Bit Extender
Gates
Plexers
Arithmetic
Selection: Constant
Facing North
Data Bits 1
Value 0x1
100%
Decd
D0
D1
D2
D3
D4
D5
D6
D7
x1
x2
x3


Logisim: main of Untitled
File Edit Project Simulate Window Help
Untitled*
main
Wiring
Splitter
Pin
Probe
Tunnel
Pull Resistor
Clock
Constant
Power
Ground
Transistor
Transmission Gate
Bit Extender
Gates
Plexers
Arithmetic
Selection: Splitter
Facing South
Fan Out 3
Bit Width In 3
Appearance Left-handed
Bit 0 0 (Right)
Bit 1 1
Bit 2 2 (Left)
100%
Decd
0
1
D0
D1
D2
D3
D4
D5
D6
D7
x1
x2
x3