LogiSim

LogiSim

- http://www.cburch.com/logisim/

Logisim

a graphical tool for designing and simulating logic circuits

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Documentation
Release History
Q & A
Comments
Links

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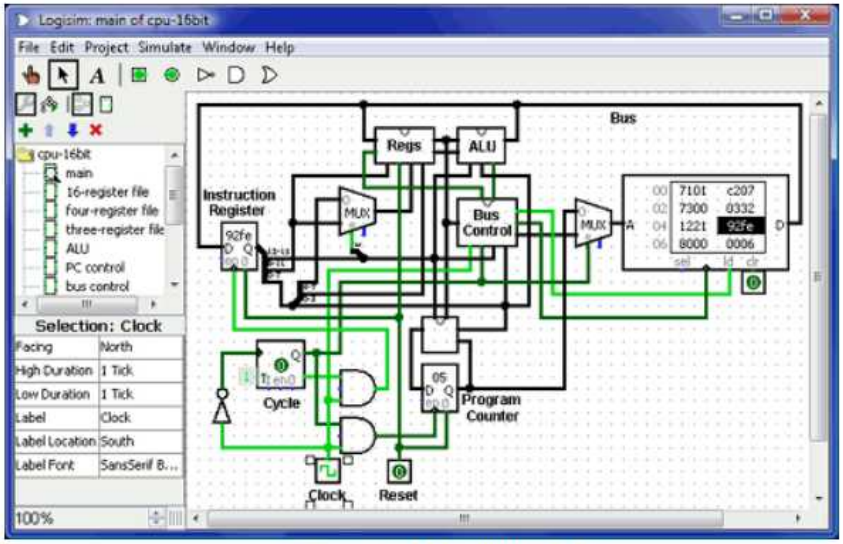
[en] English
[es] español
[pt] Português
[ru] Русский



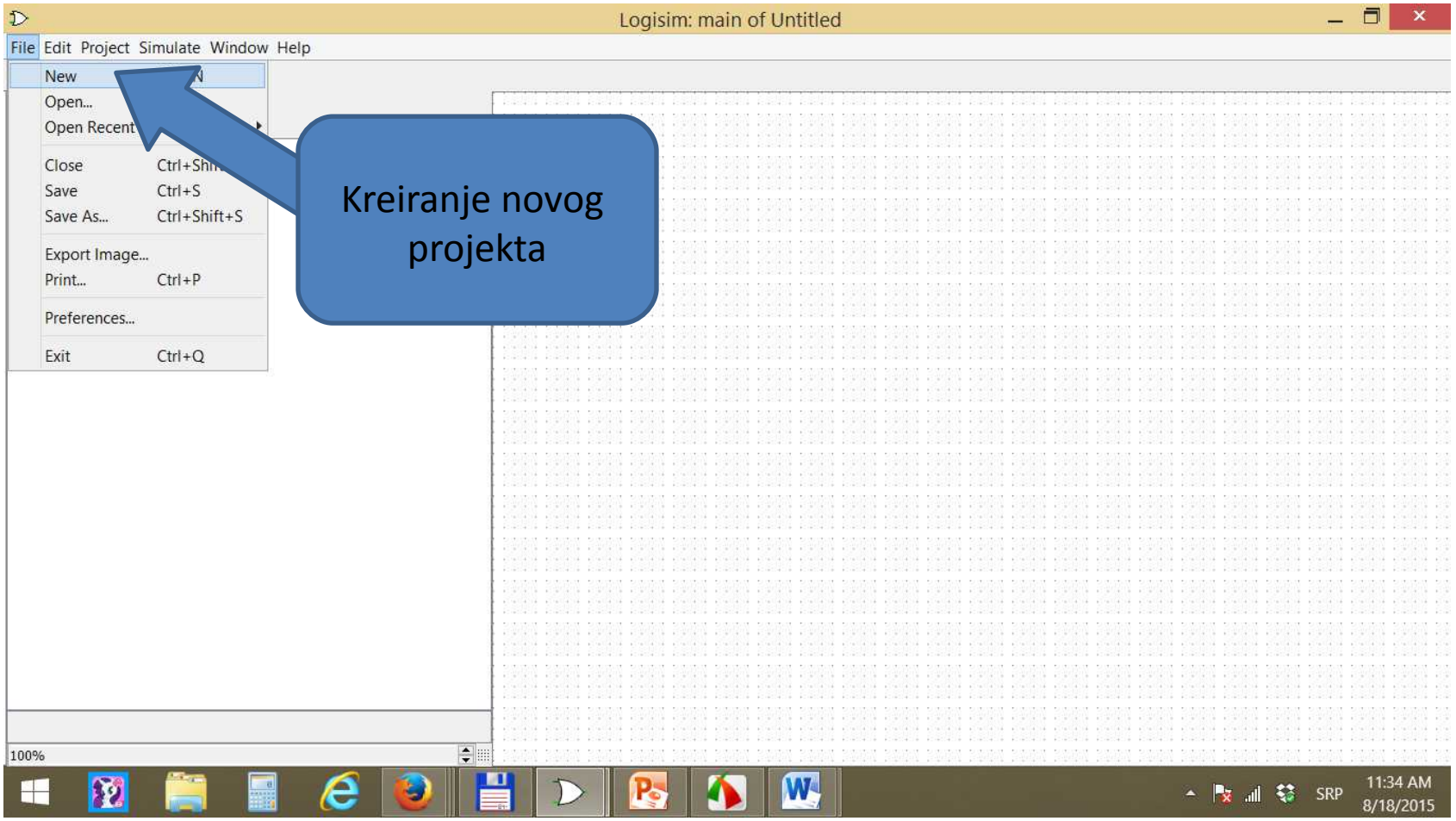
Screen shot of Logisim 2.7.0

Note: Further Logisim development is suspended indefinitely. [More information] (11 Oct 2014)

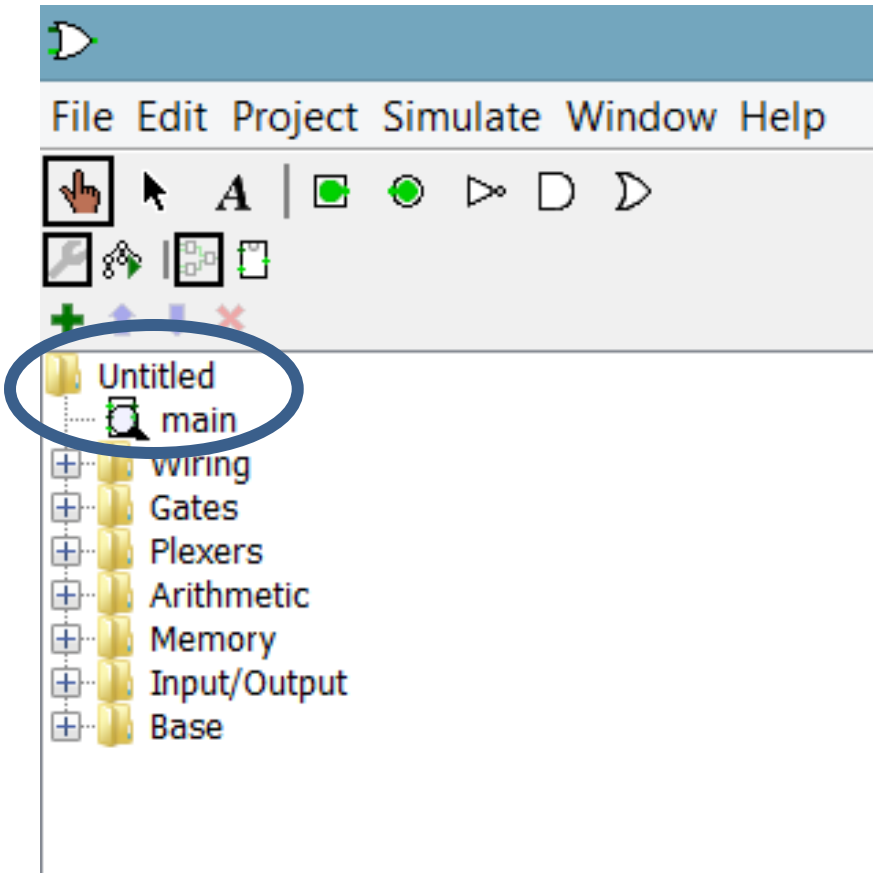
Logisim is an educational tool for designing and simulating digital logic circuits. With its simple toolt simulation of circuits as you build them, it is simple enough to facilitate learning the most basic conce

Logisim

- Pokretanje pod Win jednostavnim klikom na Logisim.exe
- Pokretanje pod Linuxom(Ubuntu)
- java –jar logisimxxx.jar


Logisim: main of Untitled
File Edit Project Simulate Window Help
New
Open...
Open Recent
Close Ctrl+Shift
Save Ctrl+S
Save As... Ctrl+Shift+S
Export Image...
Print... Ctrl+P
Preferences...
Exit Ctrl+Q
Kreiranje novog projekta
100%
SRP
11:34 AM
8/18/2015

Logisim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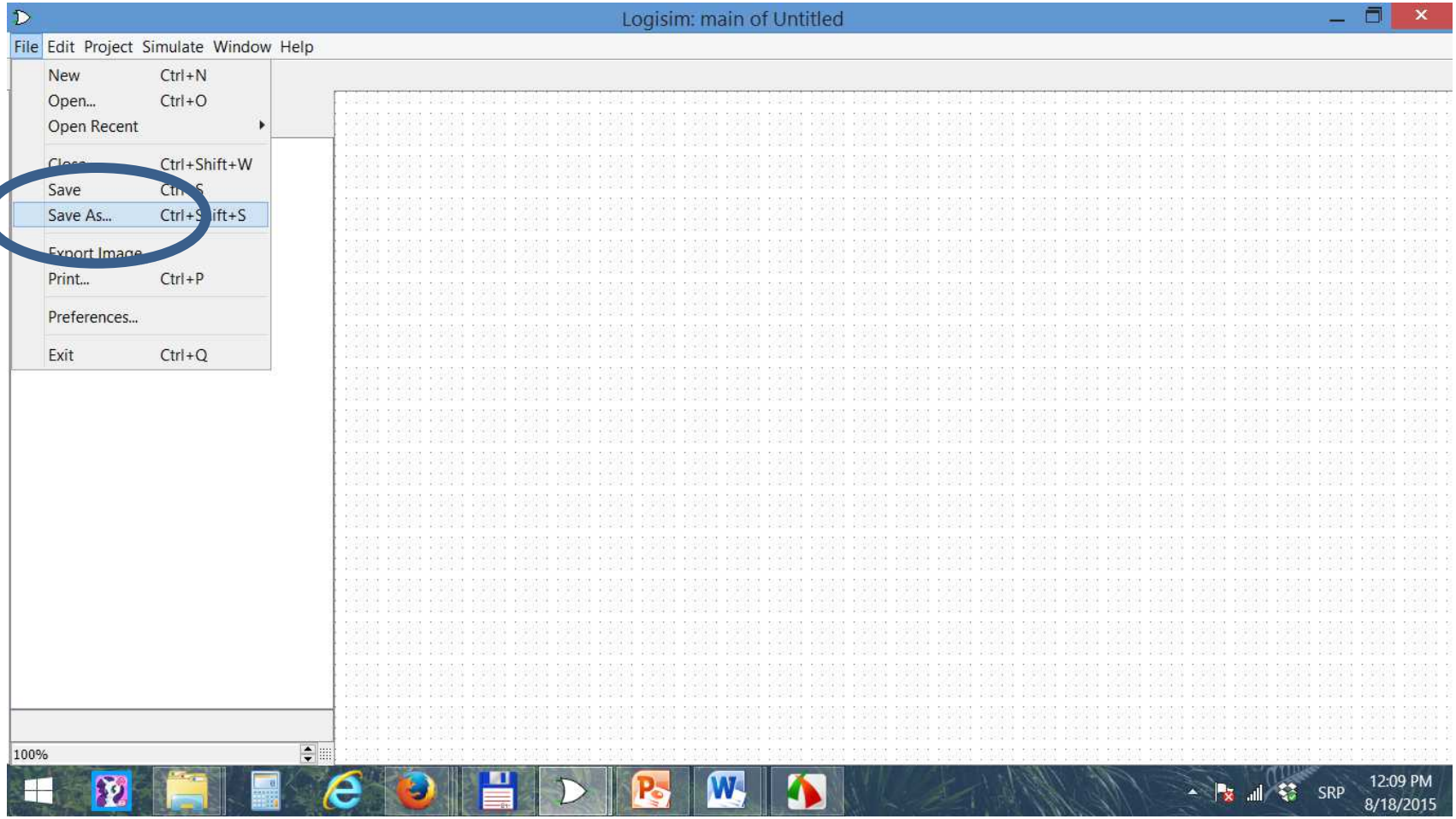
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base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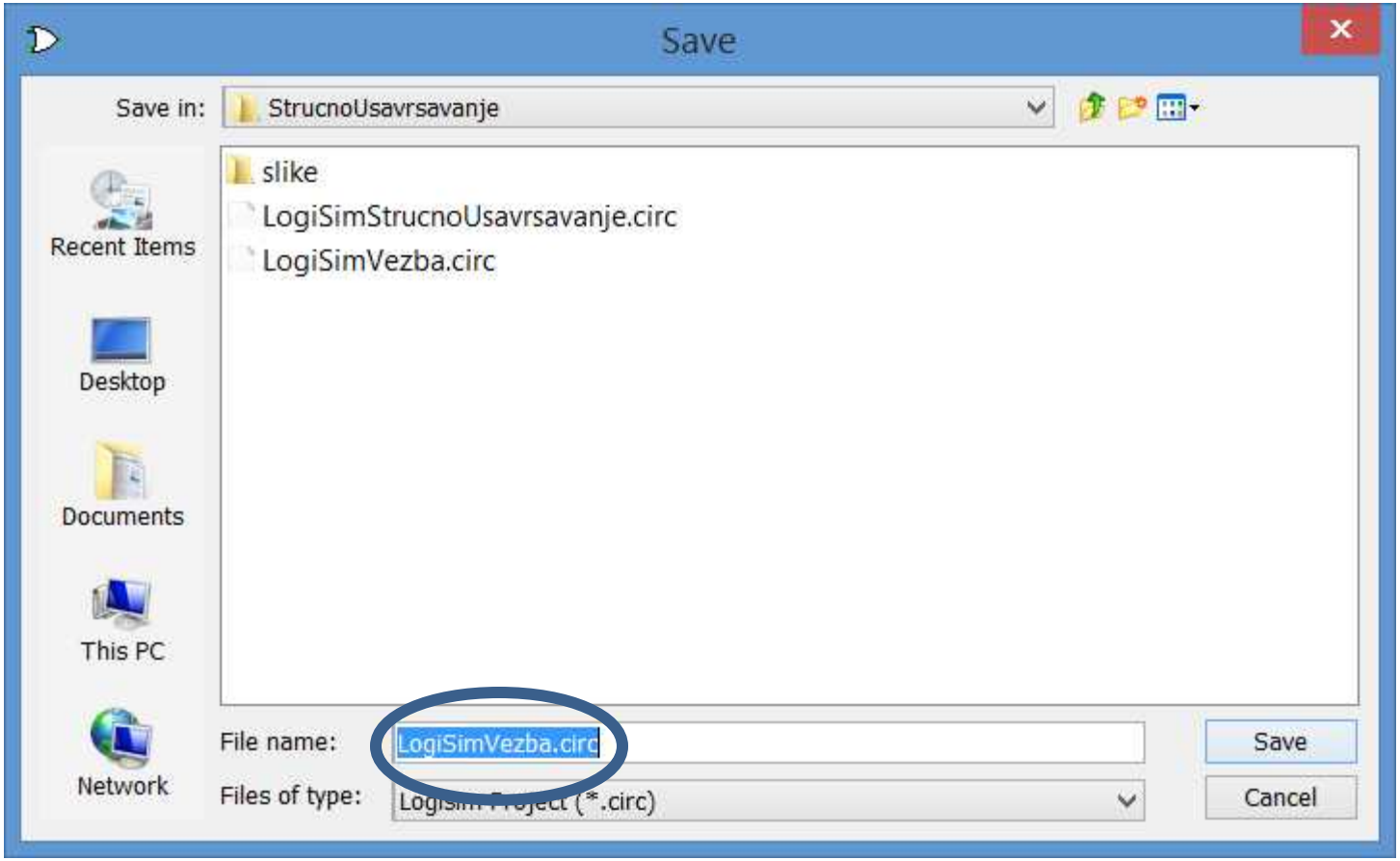
8/18/2015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StrucnoUsavrsavanje
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Desktop
Documents
This PC
Network
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Files of type:
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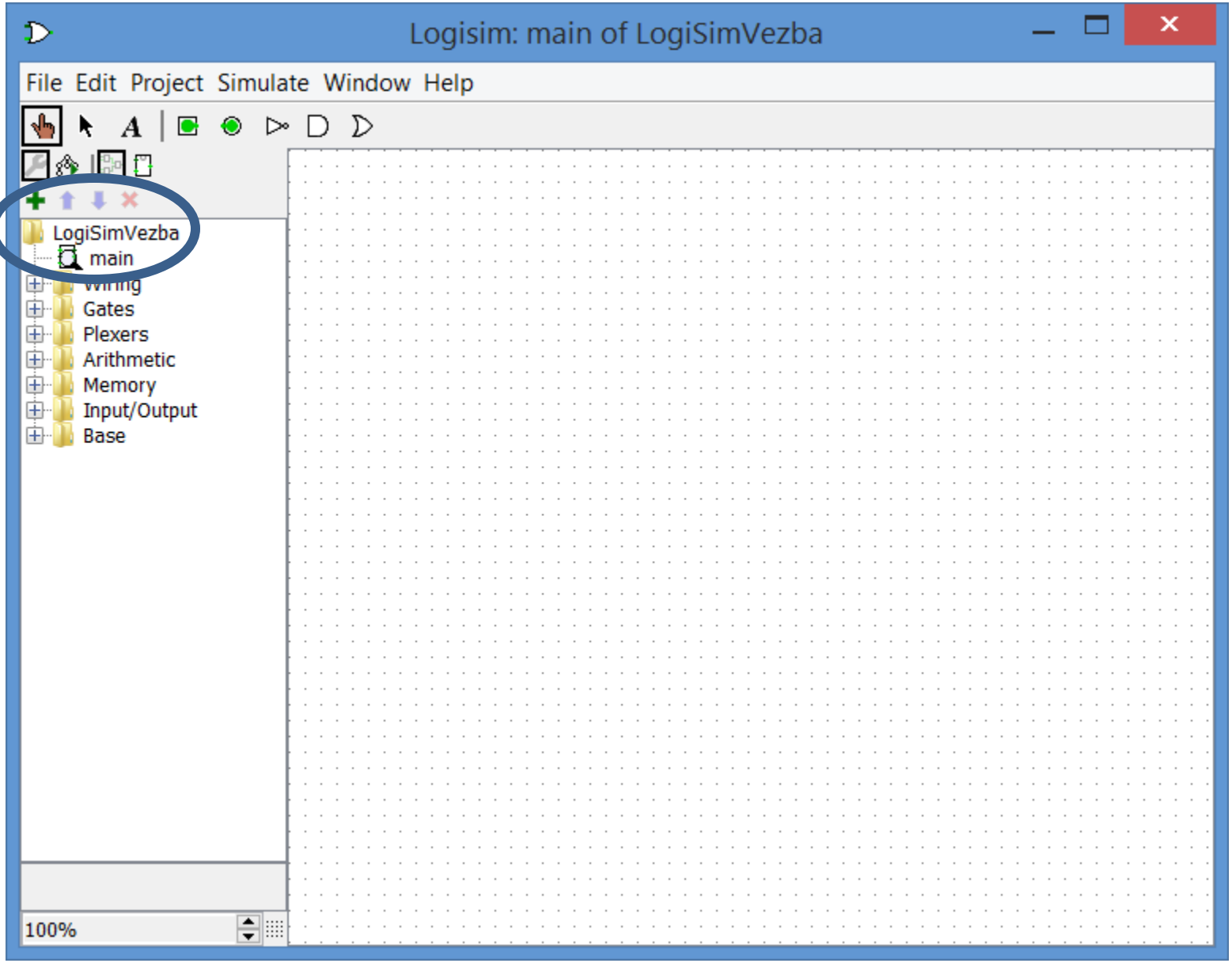
Cancel


Logisim: main of LogiSimVezba
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LogiSimVezba
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
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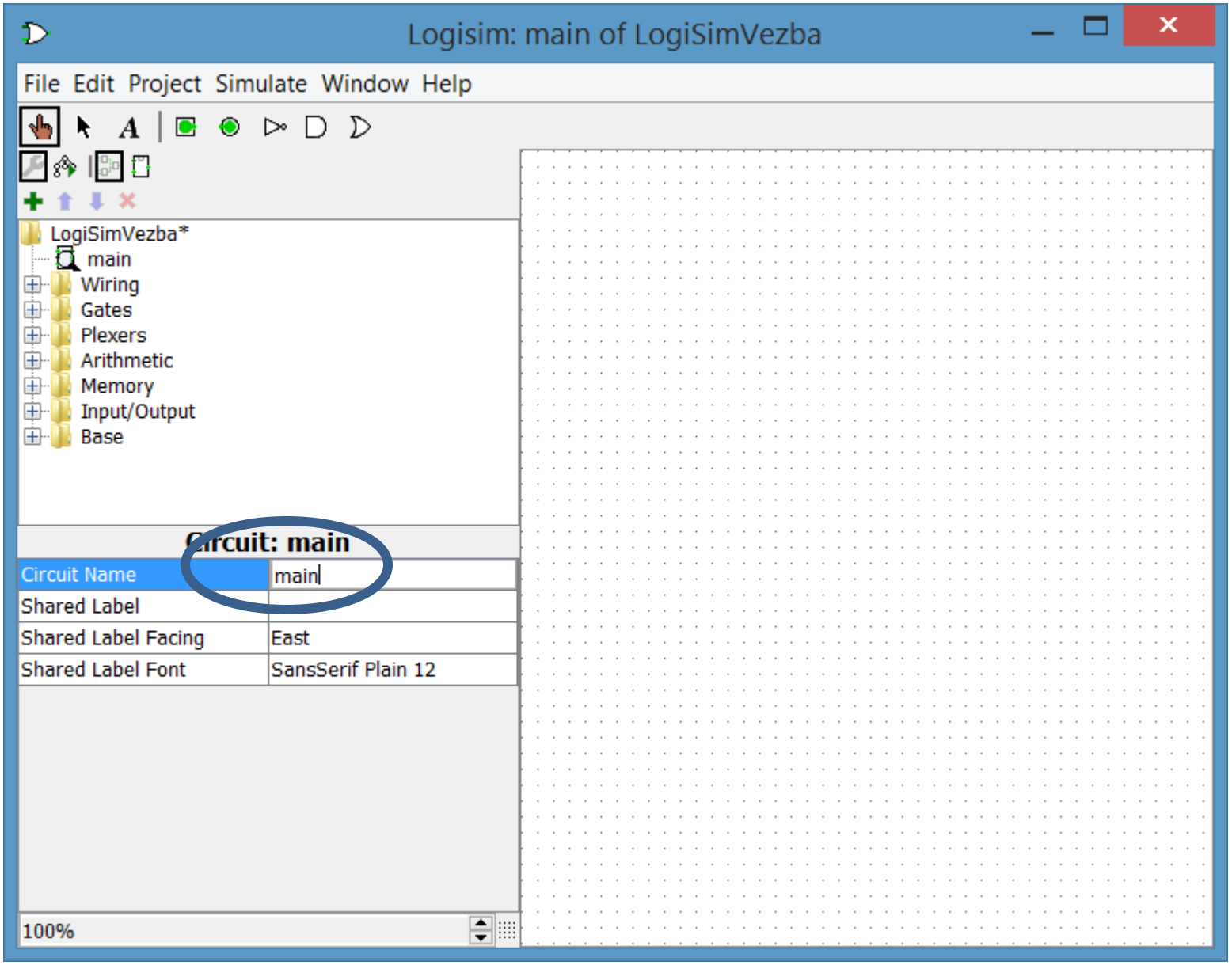
Logisim


Logisim: main of LogiSimVezba
File Edit Project Simulate Window Help
LogiSimVezba*
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Circuit: main
Circuit Name
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Shared Label
Shared Label Facing
East
Shared Label Font
SansSerif Plain 12
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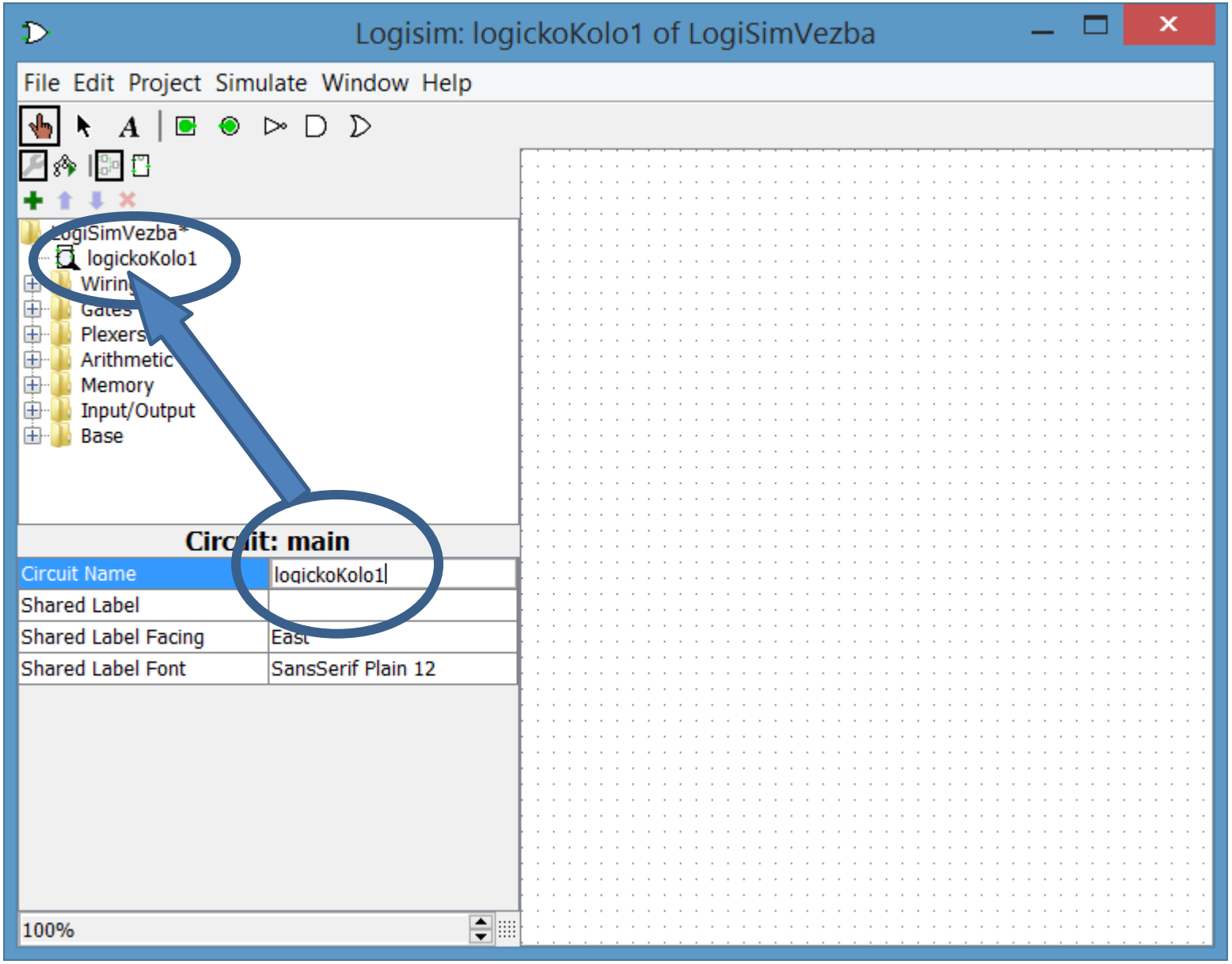
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LogiSimVezba*
logickoKolo1
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
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East
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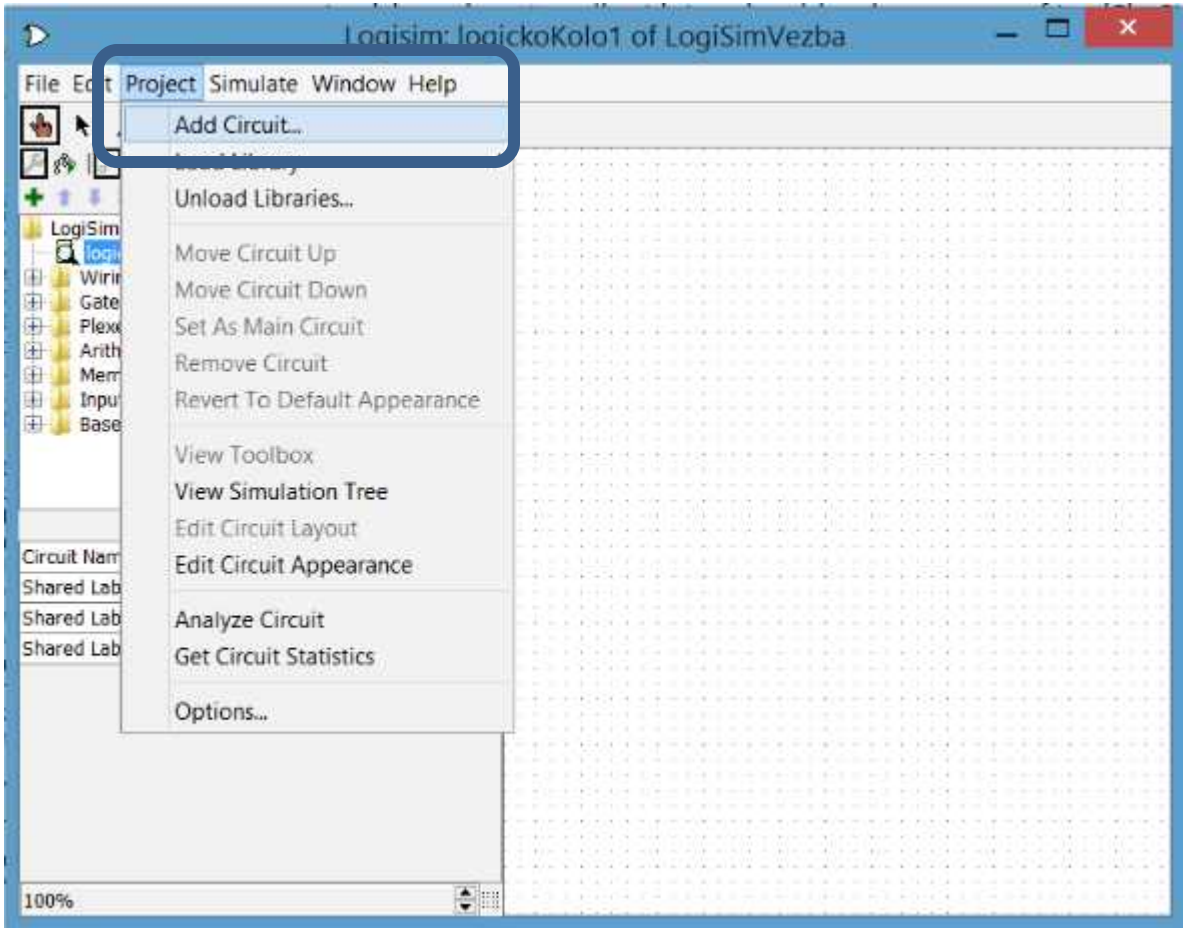
Logisim: logickoKolo1 of LogiSimVezba
File Edit Project Simulate Window Help
Add Circuit...
Unload Libraries...
Move Circuit Up
Move Circuit Down
Set As Main Circuit
Remove Circuit
Revert To Default Appearance
View Toolbox
View Simulation Tree
Edit Circuit Layout
Edit Circuit Appearance
Analyze Circuit
Get Circuit Statistics
Options...
LogiSim
Circuit Nam
Shared Lab
Shared Lab
Shared Lab
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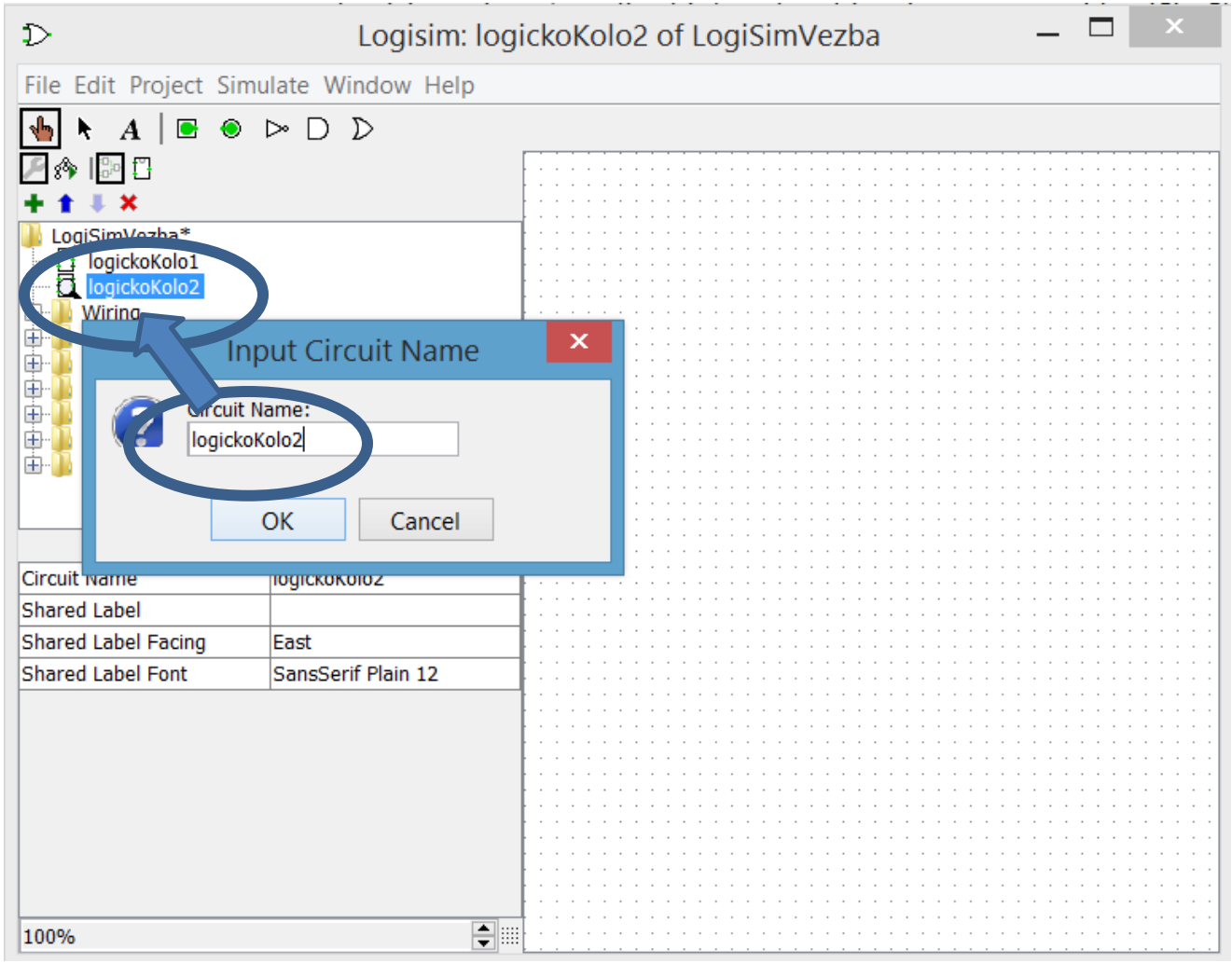
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LogiSimVezba*
logickoKolo1
logickoKolo2
Wiring
Input Circuit Name
Circuit Name:
logickoKolo2
OK
Cancel
Circuit Name
logickoKolo2
Shared Label
Shared Label Facing
East
Shared Label Font
SansSerif Plain 12
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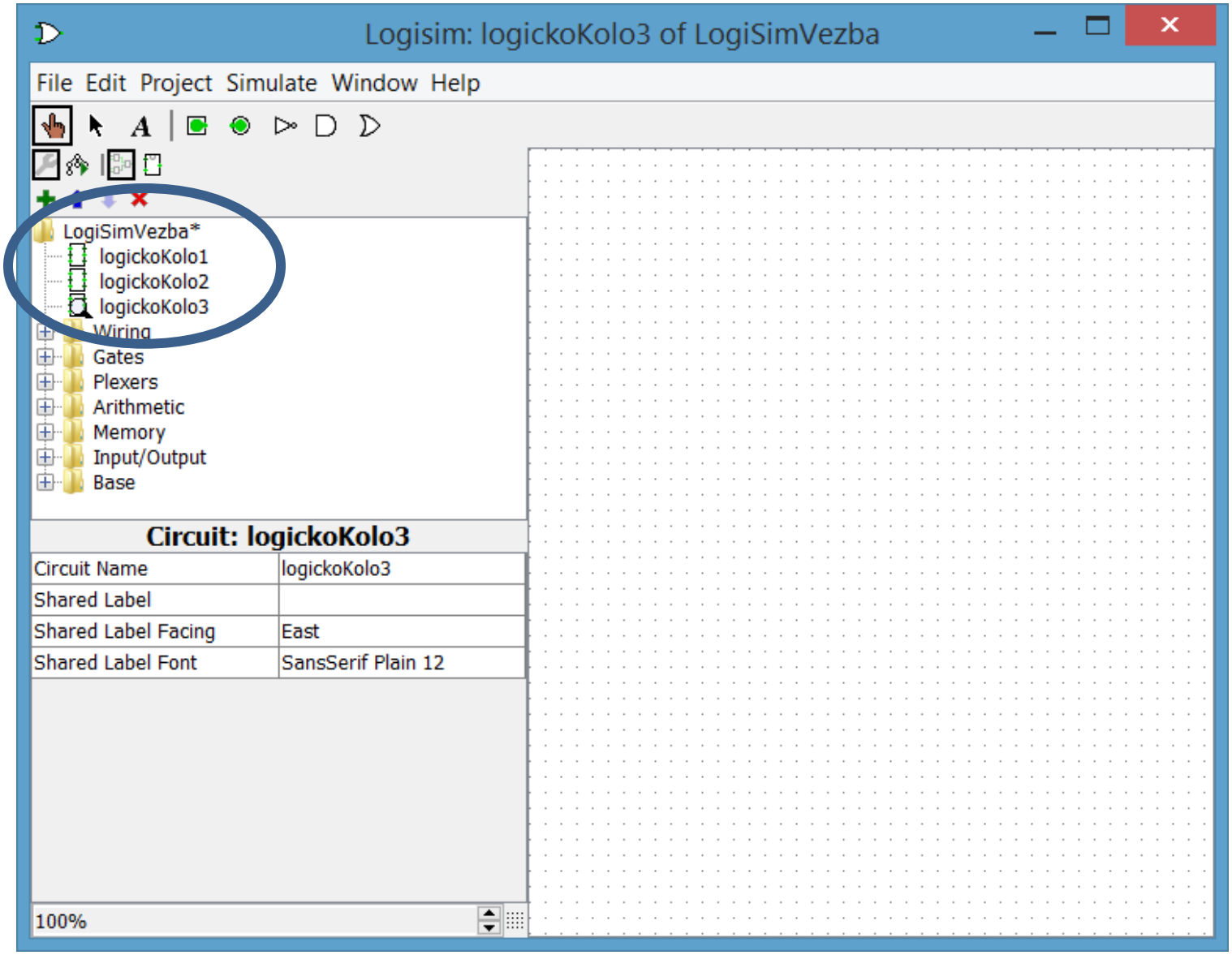
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LogiSimVezba*
logickoKolo1
logickoKolo2
logickoKolo3
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Circuit: logickoKolo3
Circuit Name
logickoKolo3
Shared Label
Shared Label Facing
East
Shared Label Font
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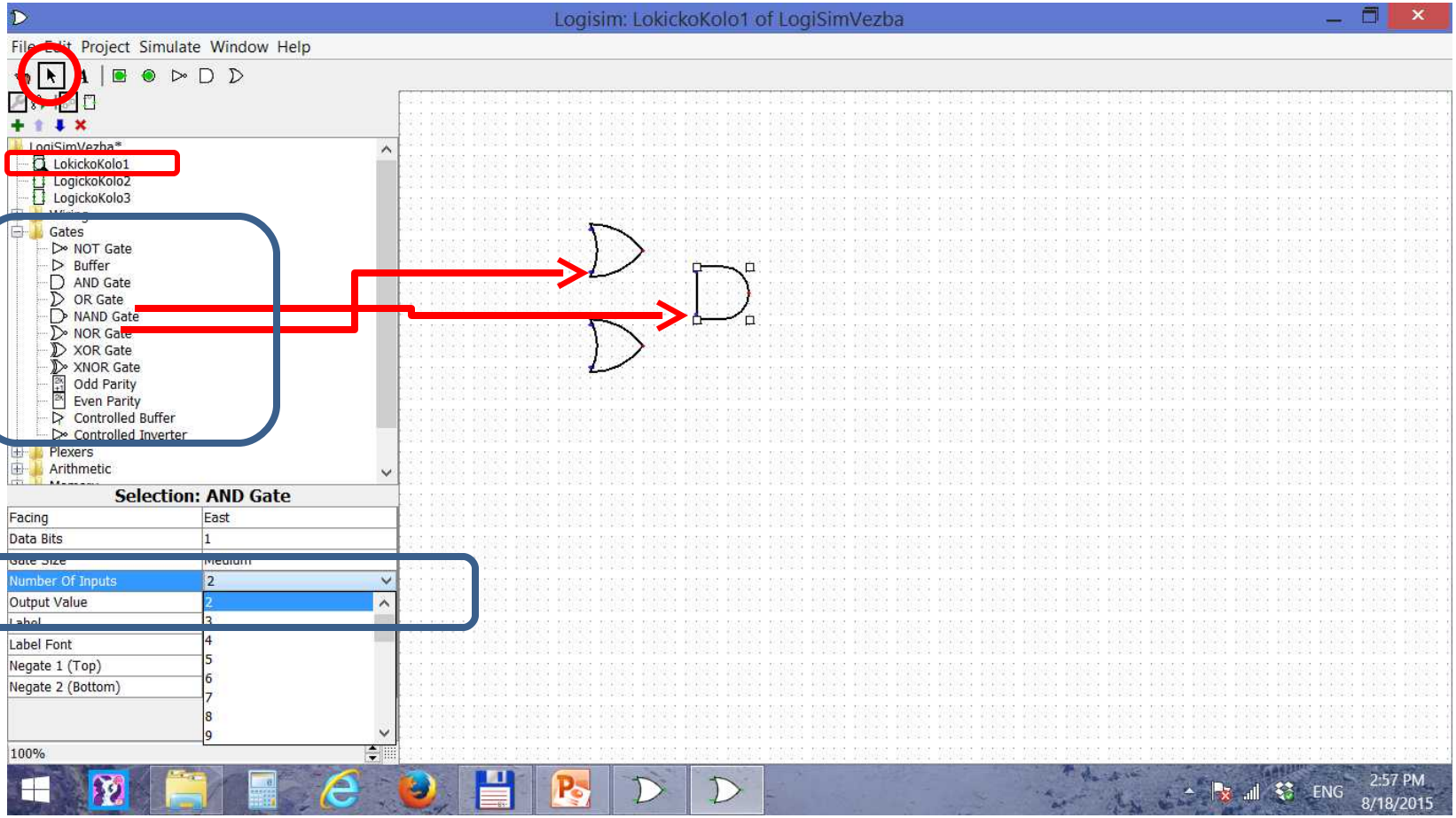
LogiSim


Logisim: LokickoKolo1 of LogiSimVezba
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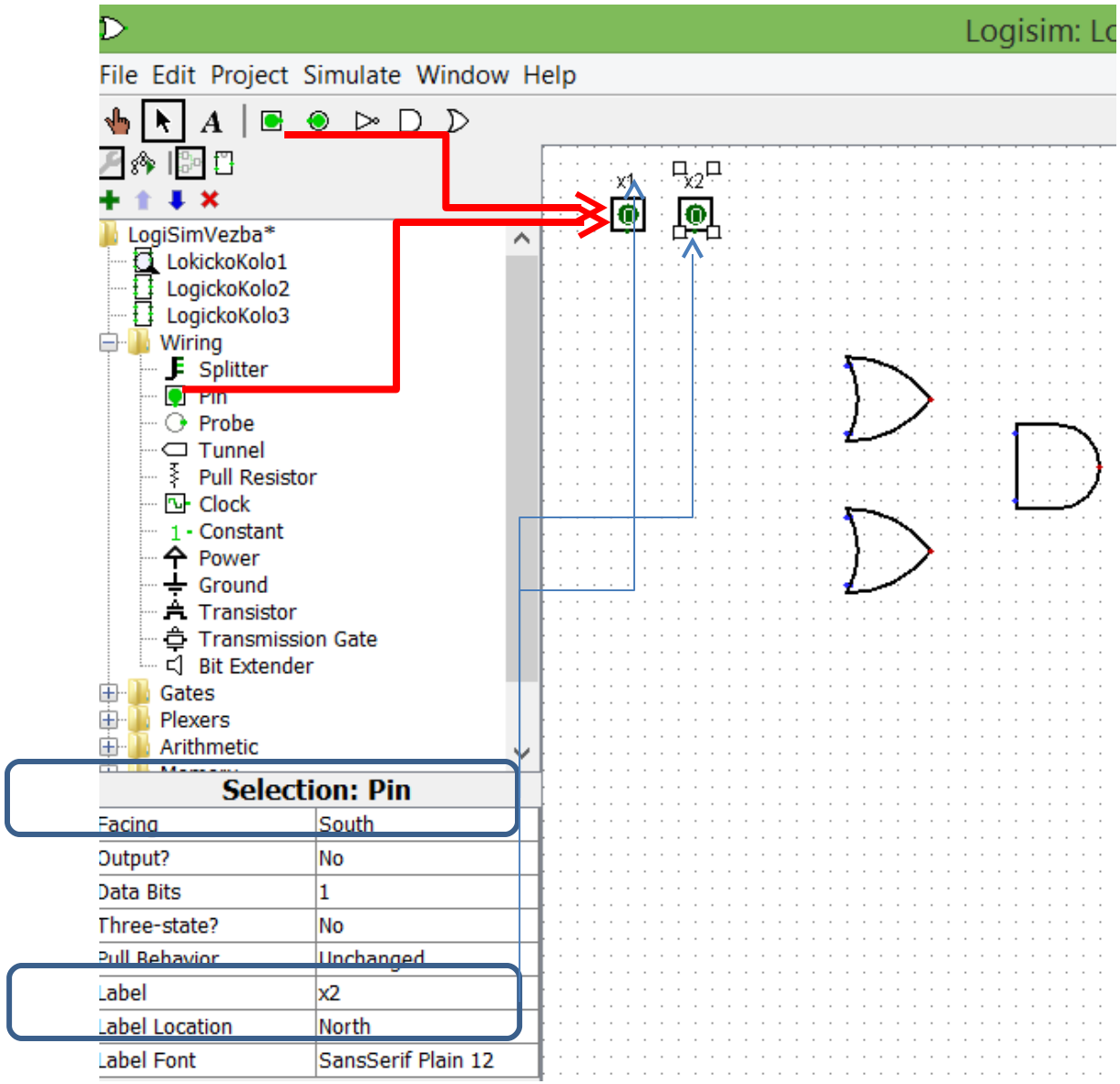
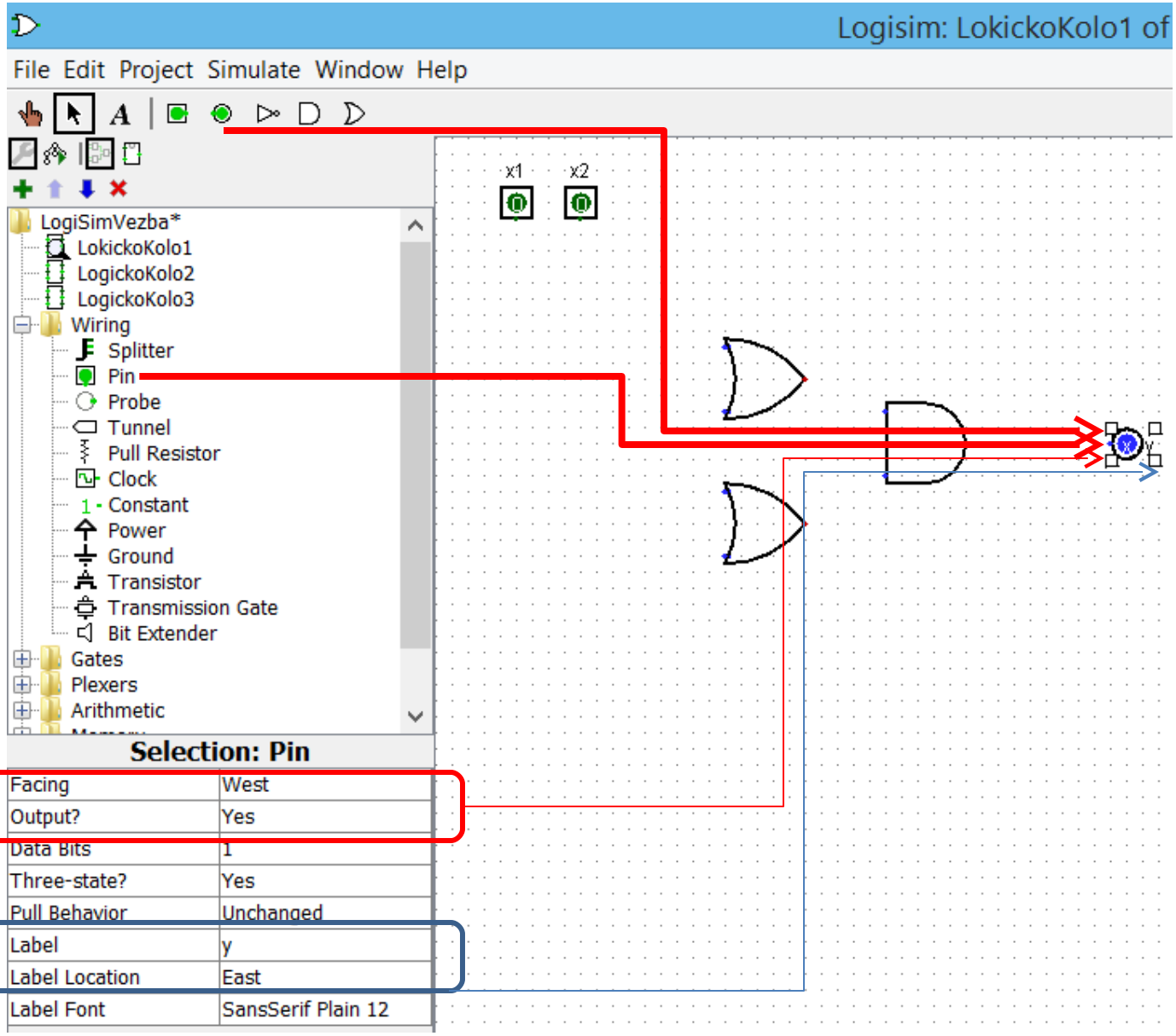
LogiSimVezba*
LokickoKolo1
LogickoKolo2
LogickoKolo3
Gates
NOT Gate
Buffer
AND Gate
OR Gate
NAND Gate
NOR Gate
XOR Gate
XNOR Gate
Odd Parity
Even Parity
Controlled Buffer
Controlled Inverter
Plexers
Arithmetic
Selection: AND Gate
Facing
East
Data Bits
1
Number Of Inputs
2
Output Value
Label Font
Negate 1 (Top)
Negate 2 (Bottom)
2
3
4
5
6
7
8
9
100%
ENG
2:57 PM
8/18/2015


Logisim: Lo
File Edit Project Simulate Window Help
LogiSimVezba*
LokickoKolo1
LogickoKolo2
LogickoKolo3
Wiring
Splitter
Pin
Probe
Tunnel
Pull Resistor
Clock
Constant
Power
Ground
Transistor
Transmission Gate
Bit Extender
Gates
Plexers
Arithmetic
x1
x2
Selection: Pin
Facing South
Output? No
Data Bits 1
Three-state? No
Pull Behavior Unchanged
Label x2
Label Location North
Label Font SansSerif Plain 12


Logisim: LokickoKolo1 of
File Edit Project Simulate Window Help
LogiSimVezba*
LokickoKolo1
LogickoKolo2
LogickoKolo3
Wiring
Splitter
Pin
Probe
Tunnel
Pull Resistor
Clock
Constant
Power
Ground
Transistor
Transmission Gate
Bit Extender
Gates
Plexers
Arithmetic
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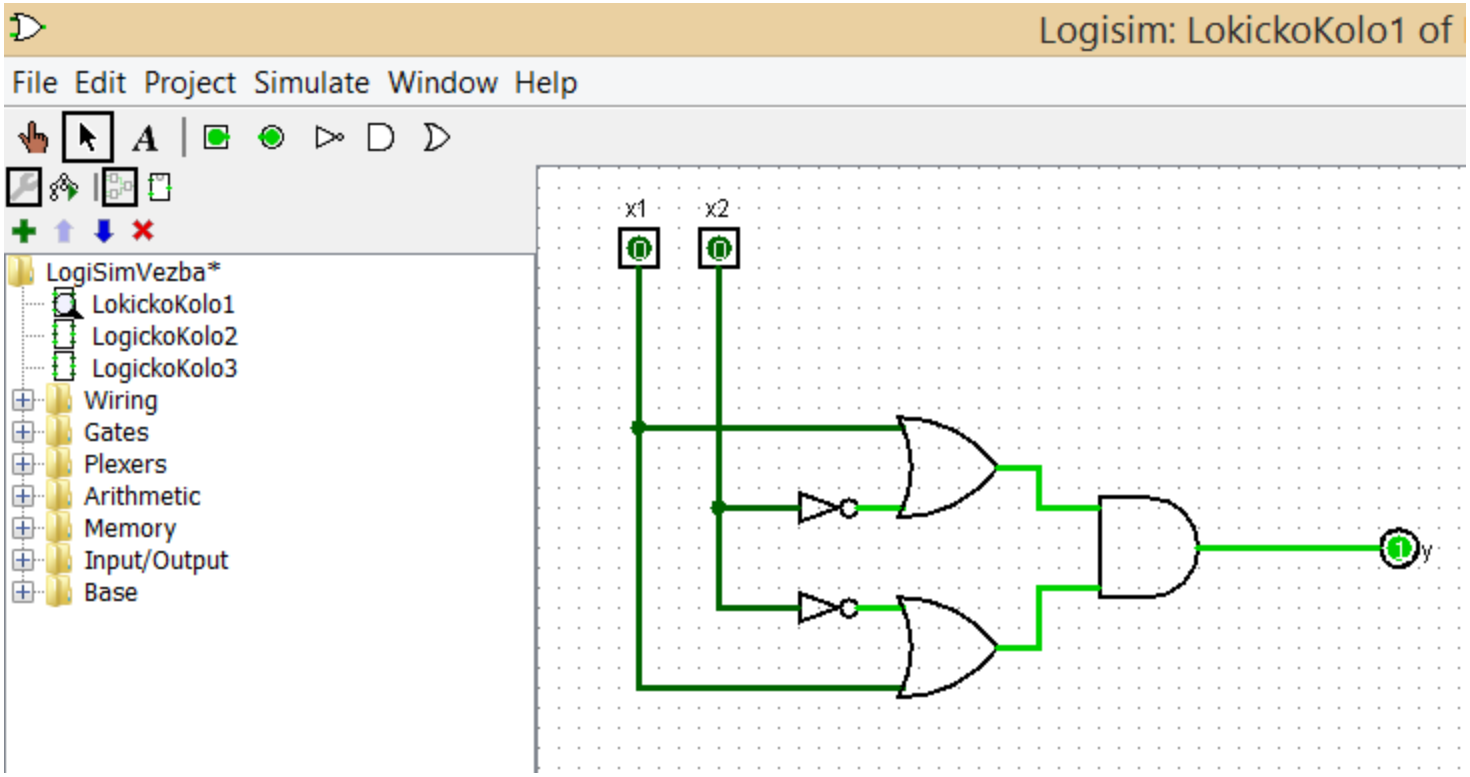
Facing West
Output? Yes
Data Bits 1
Three-state? Yes
Pull Behavior Unchanged
Label y
Label Location East
Label Font SansSerif Plain 12
x1
x2
y


Logisim: LokickoKolo1 of
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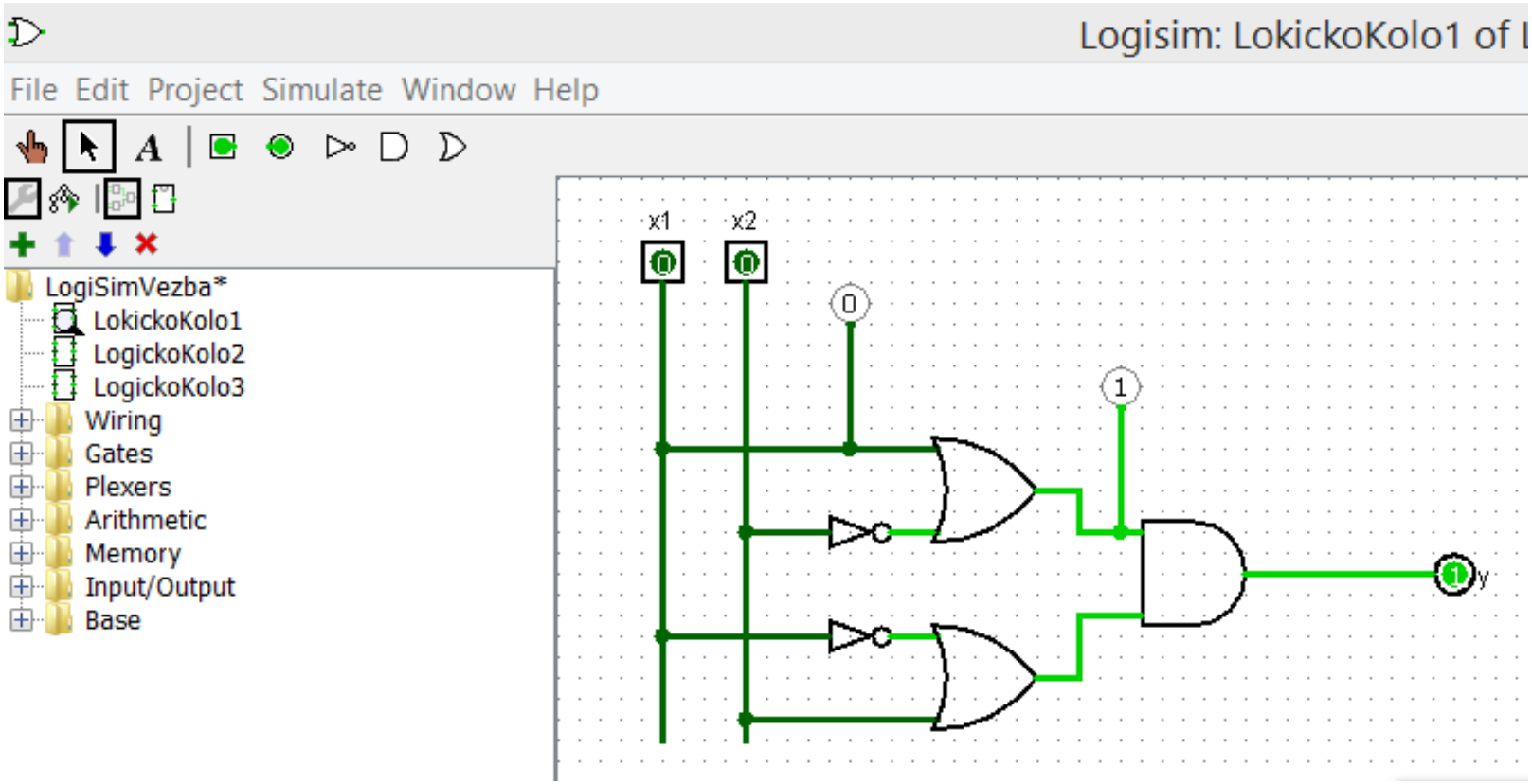
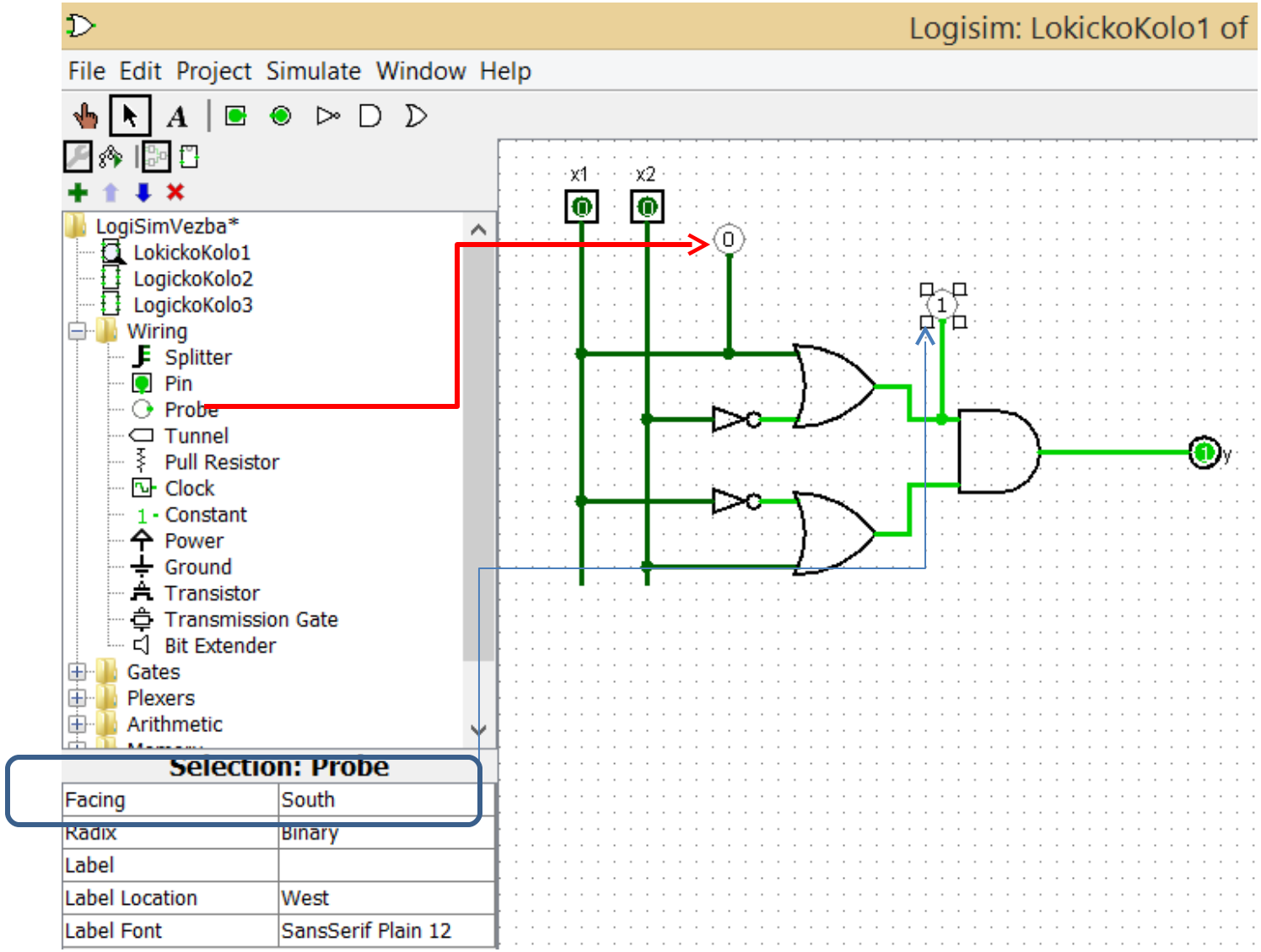
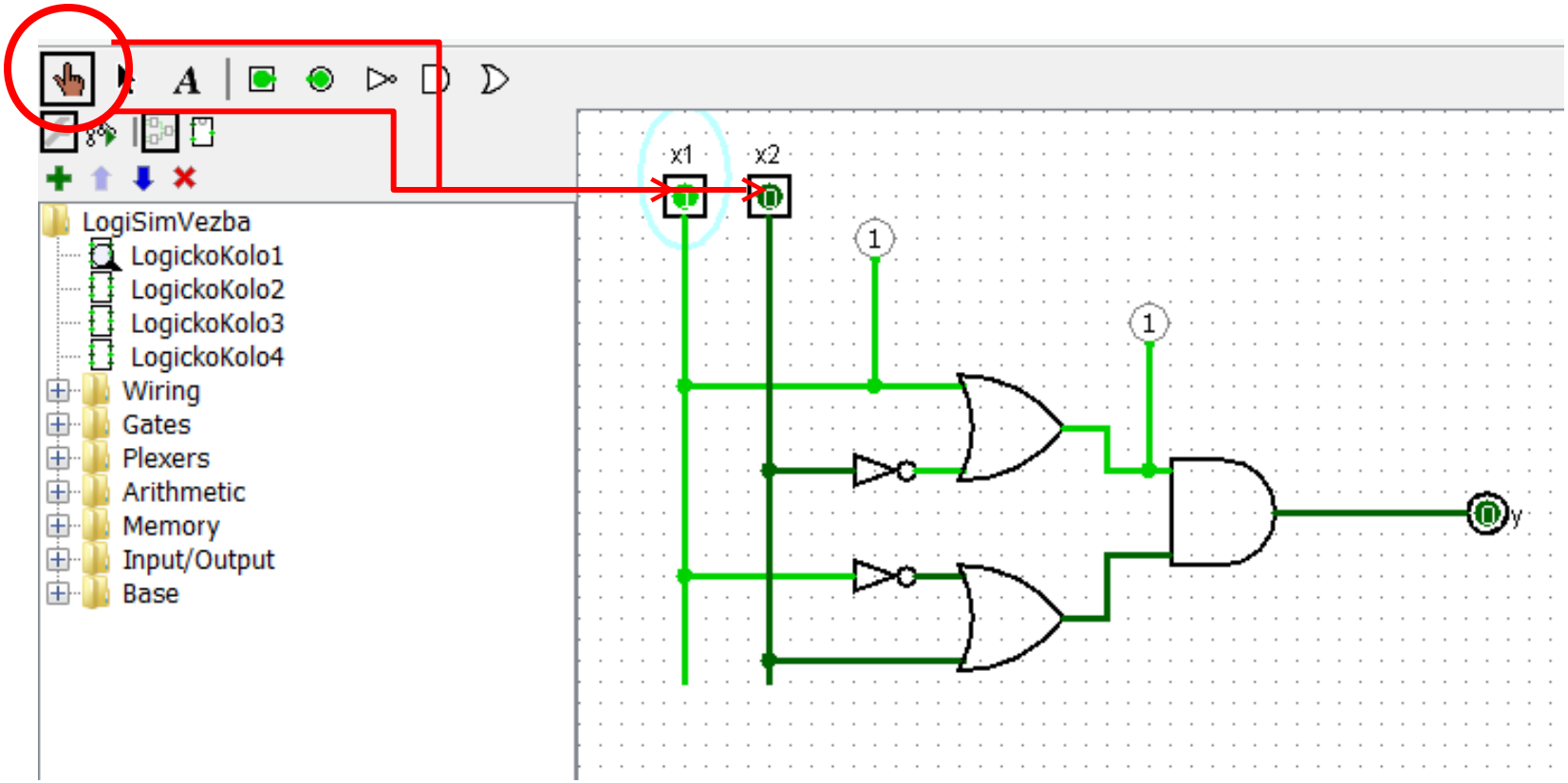
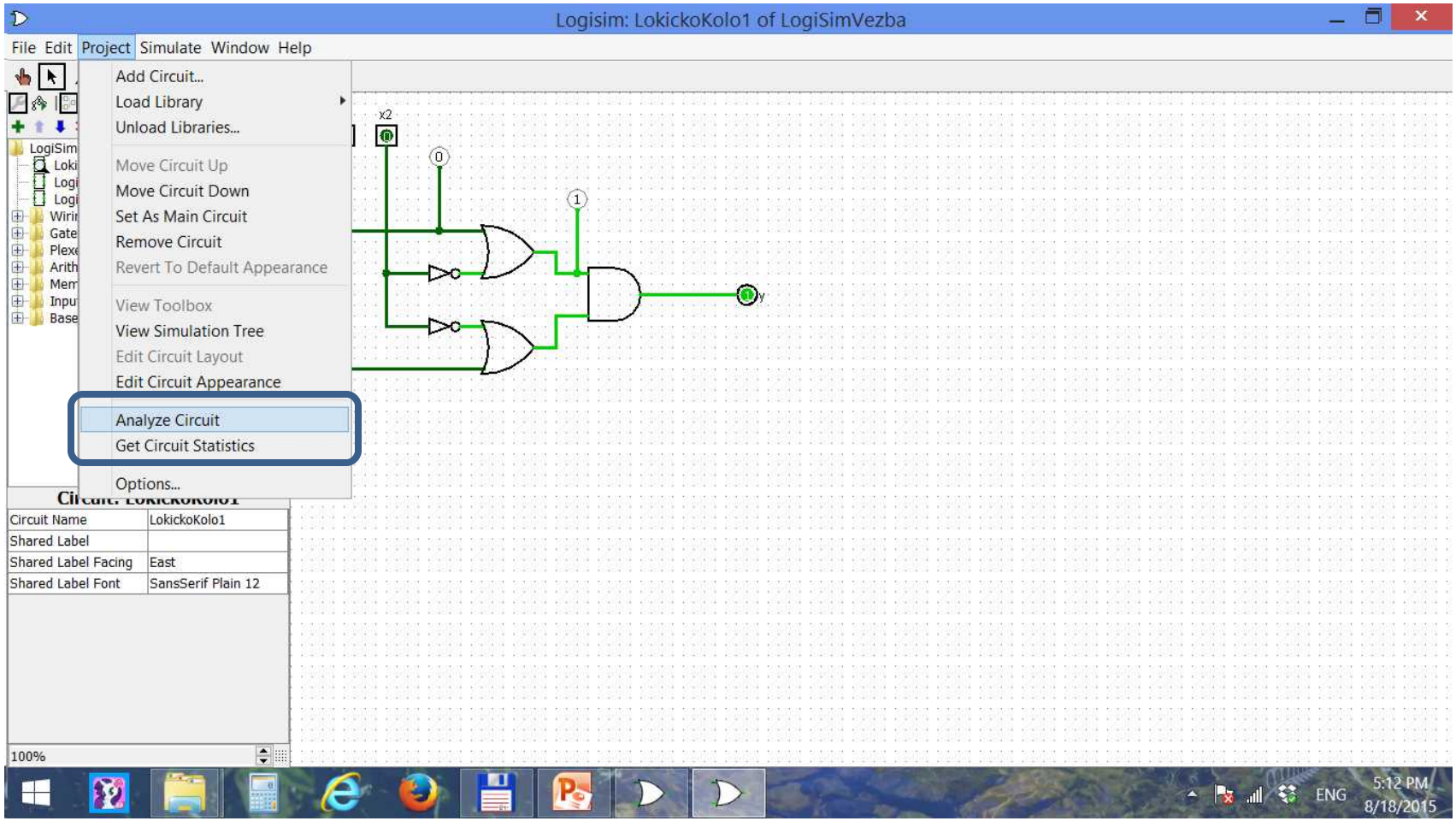
LogiSimVezba*
LokickoKolo1
LogickoKolo2
LogickoKolo3
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
x1
x2
y


Logisim: LokickoKolo1 of
File Edit Project Simulate Window Help
LogiSimVezba*
LokickoKolo1
LogickoKolo2
LogickoKolo3
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
x1
x2
0
1
y


Logisim: LokickoKolo1 of
File Edit Project Simulate Window Help
LogiSimVezba*
LokickoKolo1
LogickoKolo2
LogickoKolo3
Wiring
Splitter
Pin
Probe
Tunnel
Pull Resistor
Clock
Constant
Power
Ground
Transistor
Transmission Gate
Bit Extender
Gates
Plexers
Arithmetic
x1
x2
0
1
y
Selection: Probe
Facing
South
Radix
Binary
Label
Label Location
West
Label Font
SansSerif Plain 12


A
LogiSimVezba
LogickoKolo1
LogickoKolo2
LogickoKolo3
LogickoKolo4
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
x1
x2
1
1
y


Logisim: LokickoKolo1 of LogiSimVezba
File Edit Project Simulate Window Help
Add Circuit...
Load Library
Unload Libraries...
Move Circuit Up
Move Circuit Down
Set As Main Circuit
Remove Circuit
Revert To Default Appearance
View Toolbox
View Simulation Tree
Edit Circuit Layout
Edit Circuit Appearance
Analyze Circuit
Get Circuit Statistics
Options...
x2
0
1
y
Circuit Name
LokickoKolo1
Shared Label
Shared Label Facing
East
Shared Label Font
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ENG
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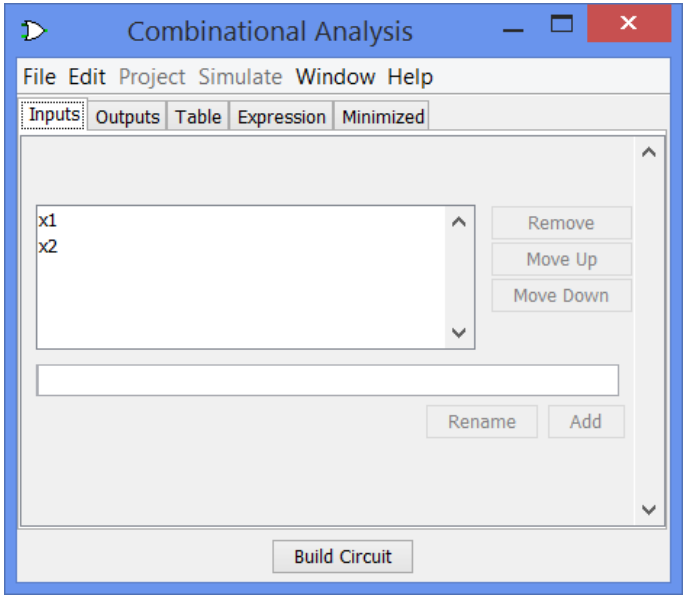
8/18/2015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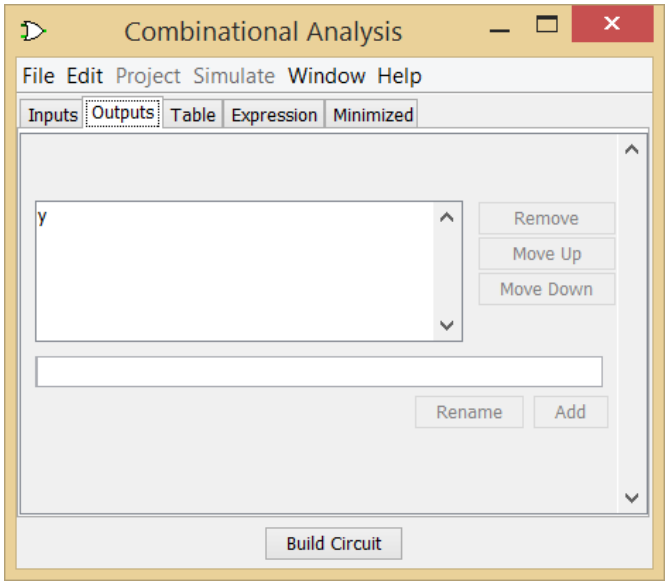
Inputs Outputs Table Expression Minimized
x1
x2
Remove
Move Up
Move Down
Rename
Add
Build Circuit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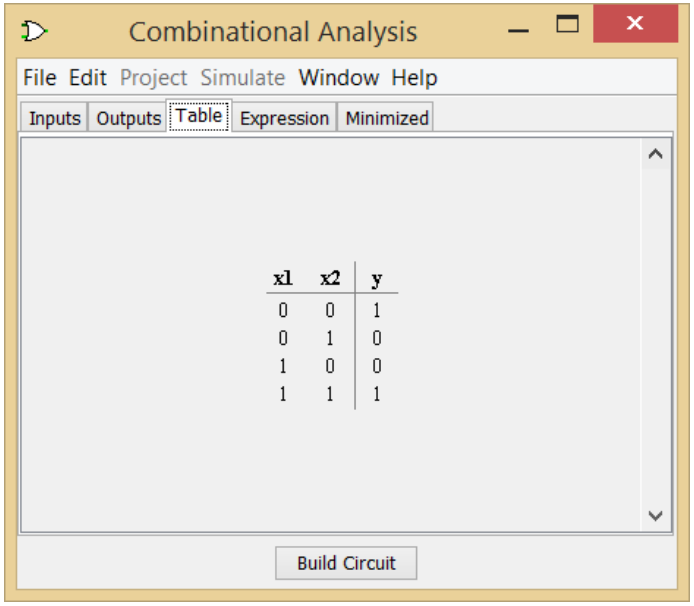
Remove
Move Up
Move Down
Rename
Add
Build Circuit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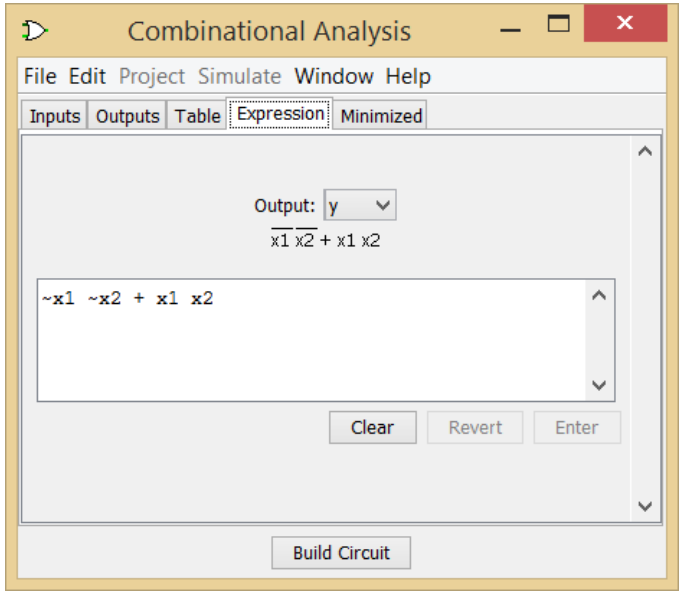
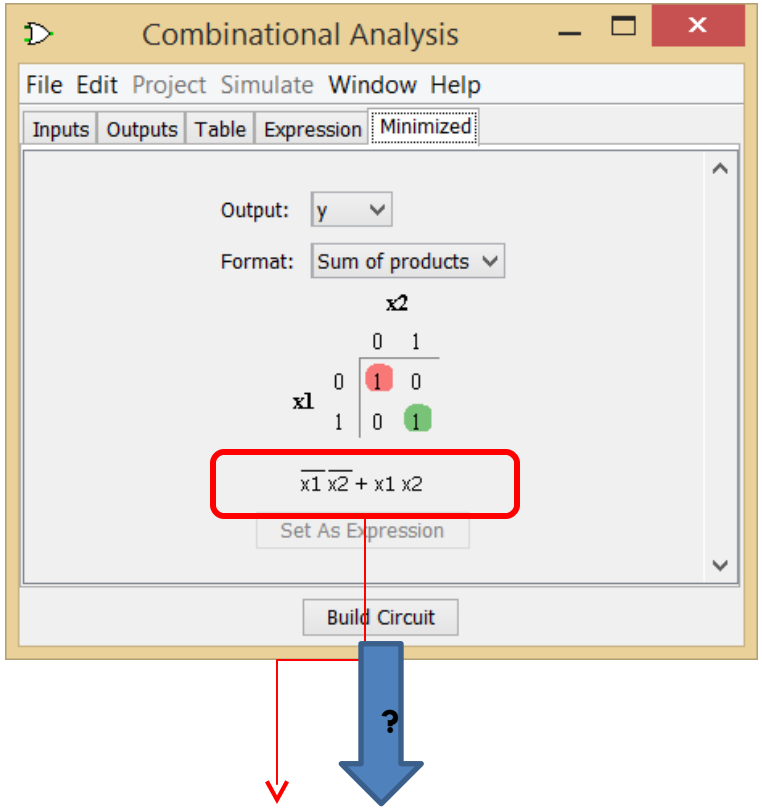
x1 x2 y
0 0 1
0 1 0
1 0 0
1 1 1
Build Circuit


Combinational Analysis
File Edit Project Simulate Window Help
Inputs Outputs Table Expression Minimized
Output: y
x1 x2 + x1 x2
~x1 ~x2 + x1 x2
Clear
Revert
Enter
Build Circuit



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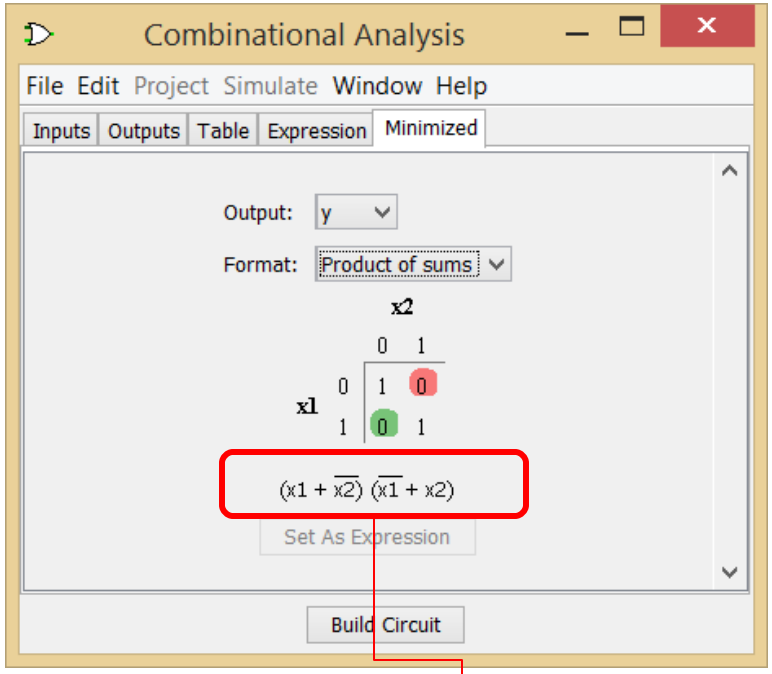

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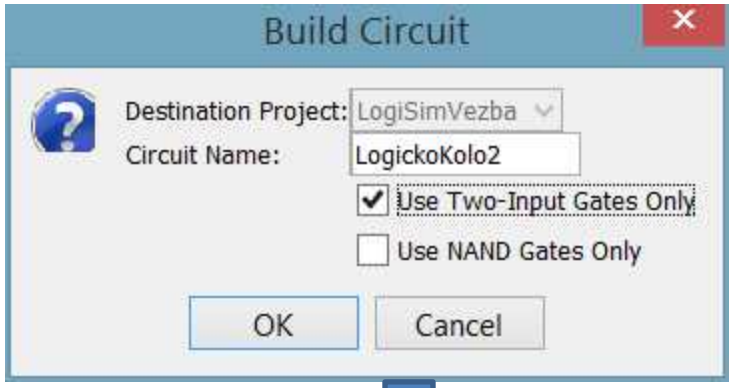
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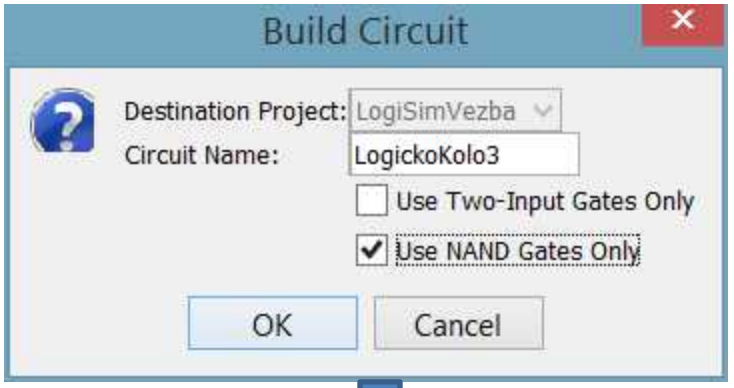
Destination Project:
LogiSimVezba
Circuit Name:
LogickoKolo2
Use Two-Input Gates Only
Use NAND Gates Only
OK
Cancel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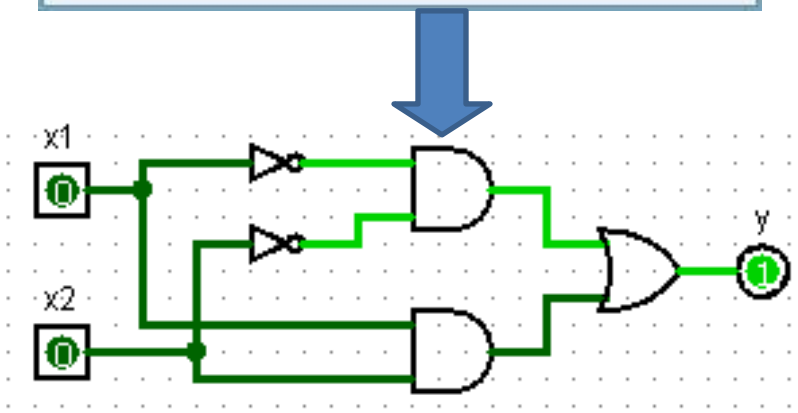
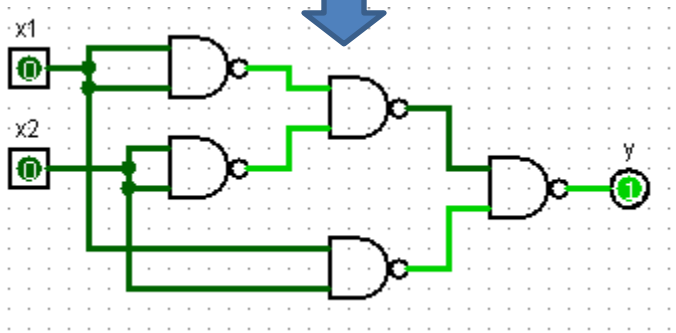
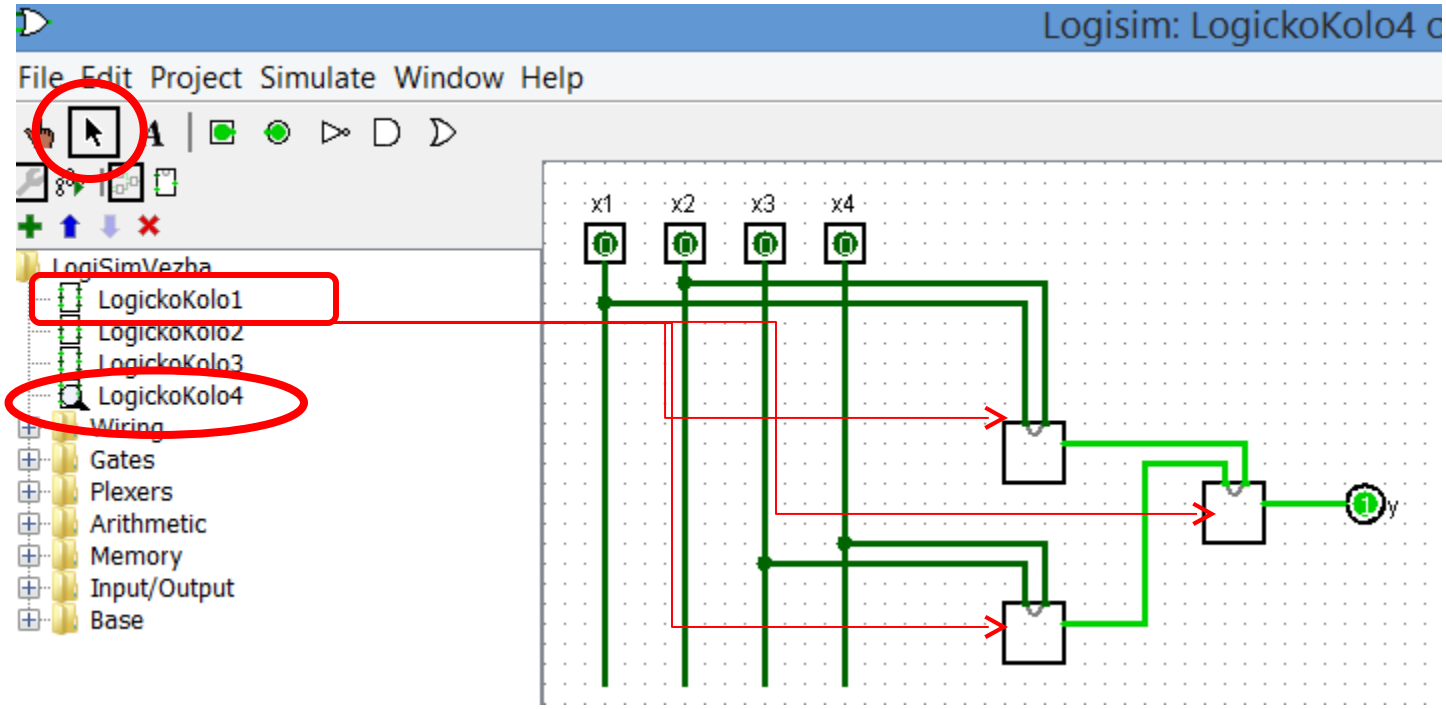
Destination Project:
LogiSimVezba
Circuit Name:
LogickoKolo3
Use Two-Input Gates Only
Use NAND Gates Only
OK
Cancel


x1
x2
y


x1
x2
y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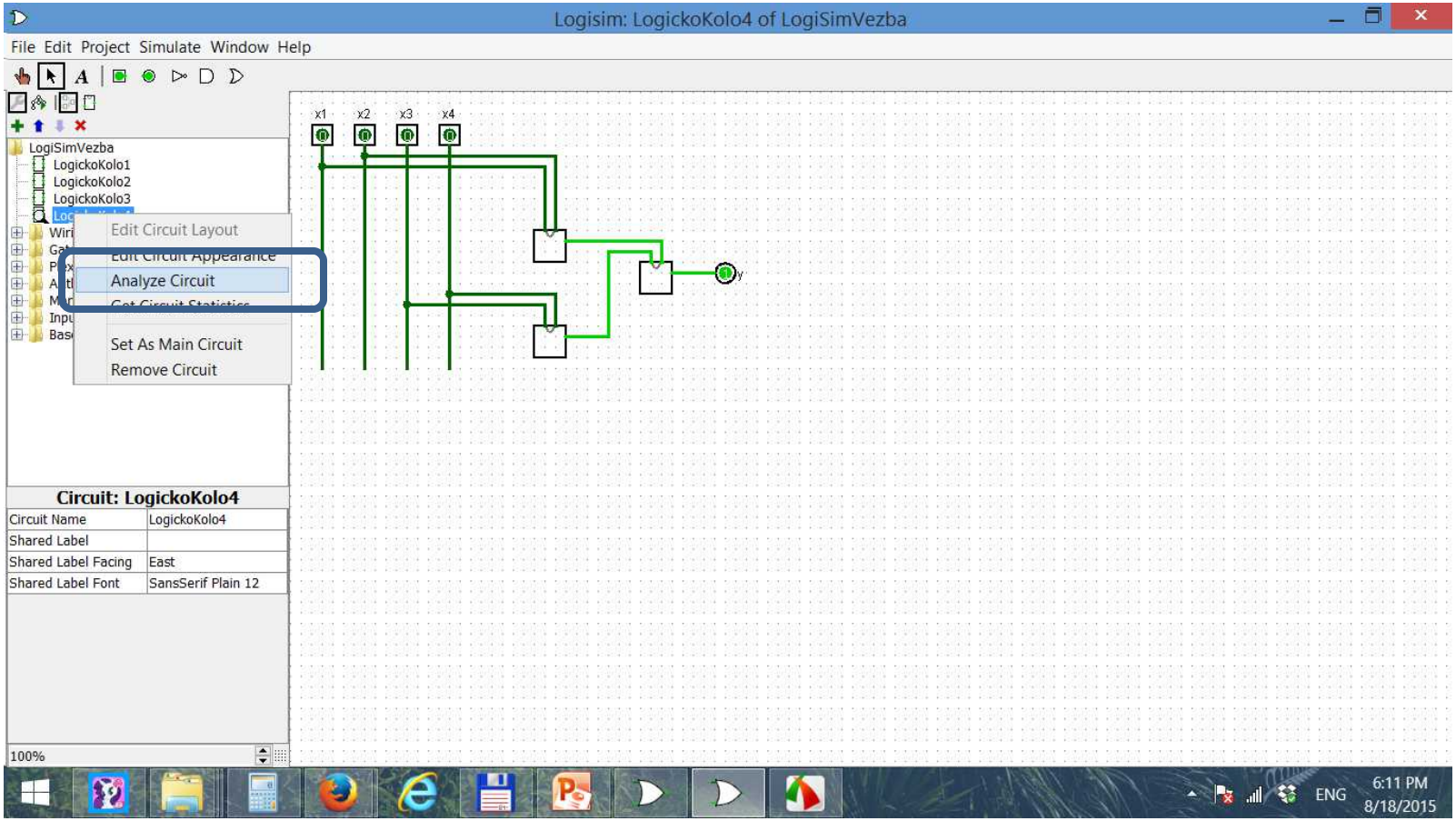
File Edit Project Simulate Window Help
LogiSimVezba
LogickoKolo1
LogickoKolo2
LogickoKolo3
LogickoKolo4
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
x1
x2
x3
x4
y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File Edit Project Simulate Window Help
LogiSimVezba
LogickoKolo1
LogickoKolo2
LogickoKolo3
Edit Circuit Layout
Analyze Circuit
Set As Main Circuit
Remove Circuit
x1
x2
x3
x4
y
Circuit: LogickoKolo4
Circuit Name
LogickoKolo4
Shared Label
Shared Label Facing
East
Shared Label Font
SansSerif Plain 12
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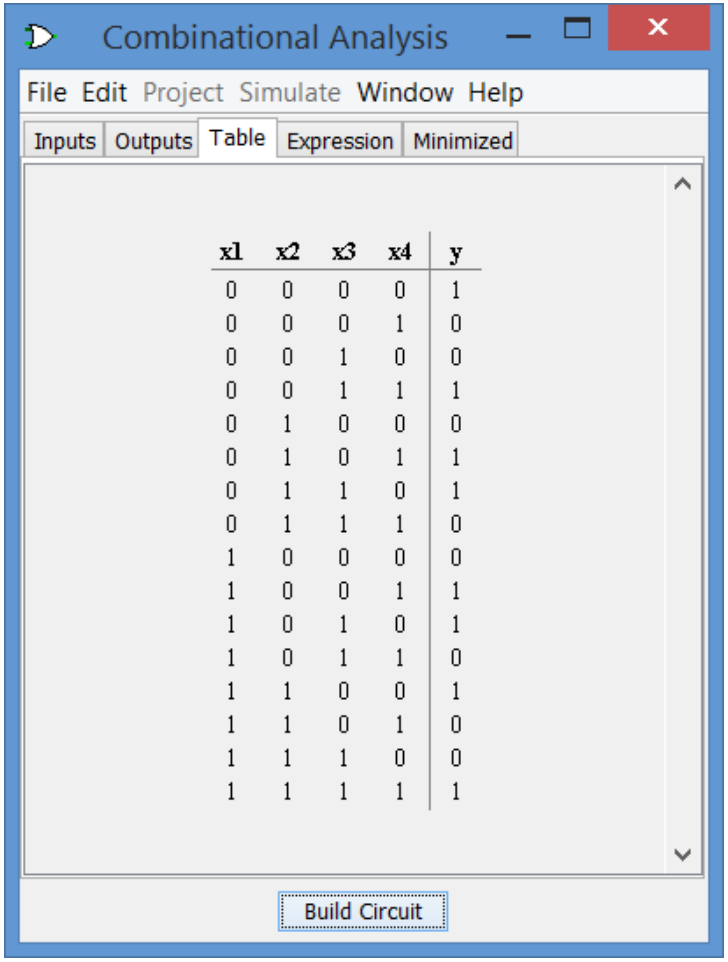
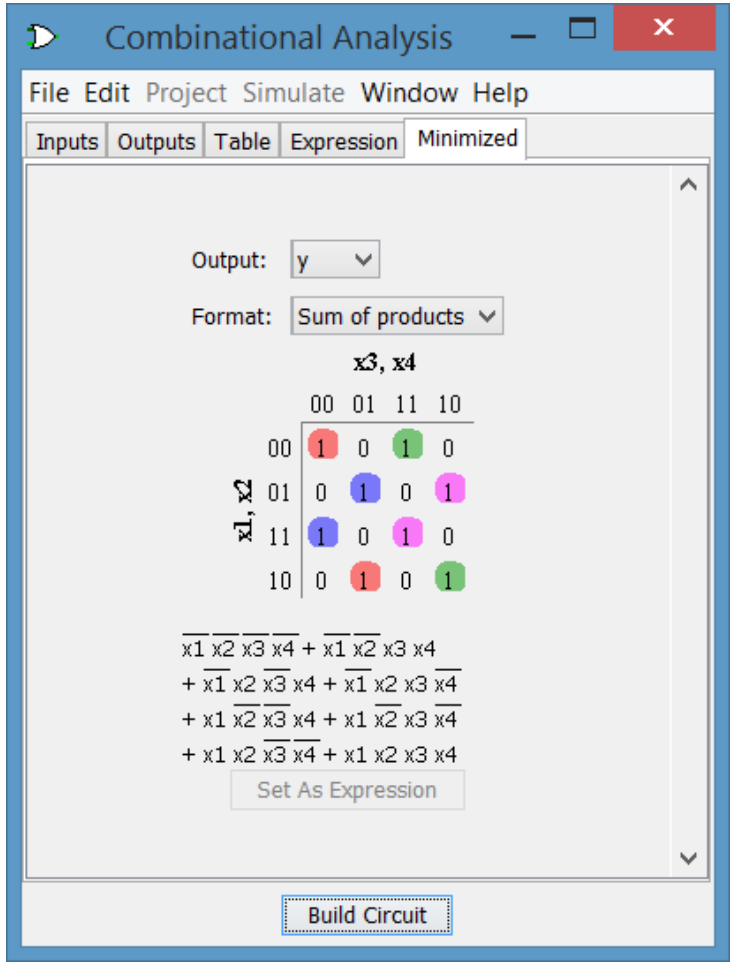
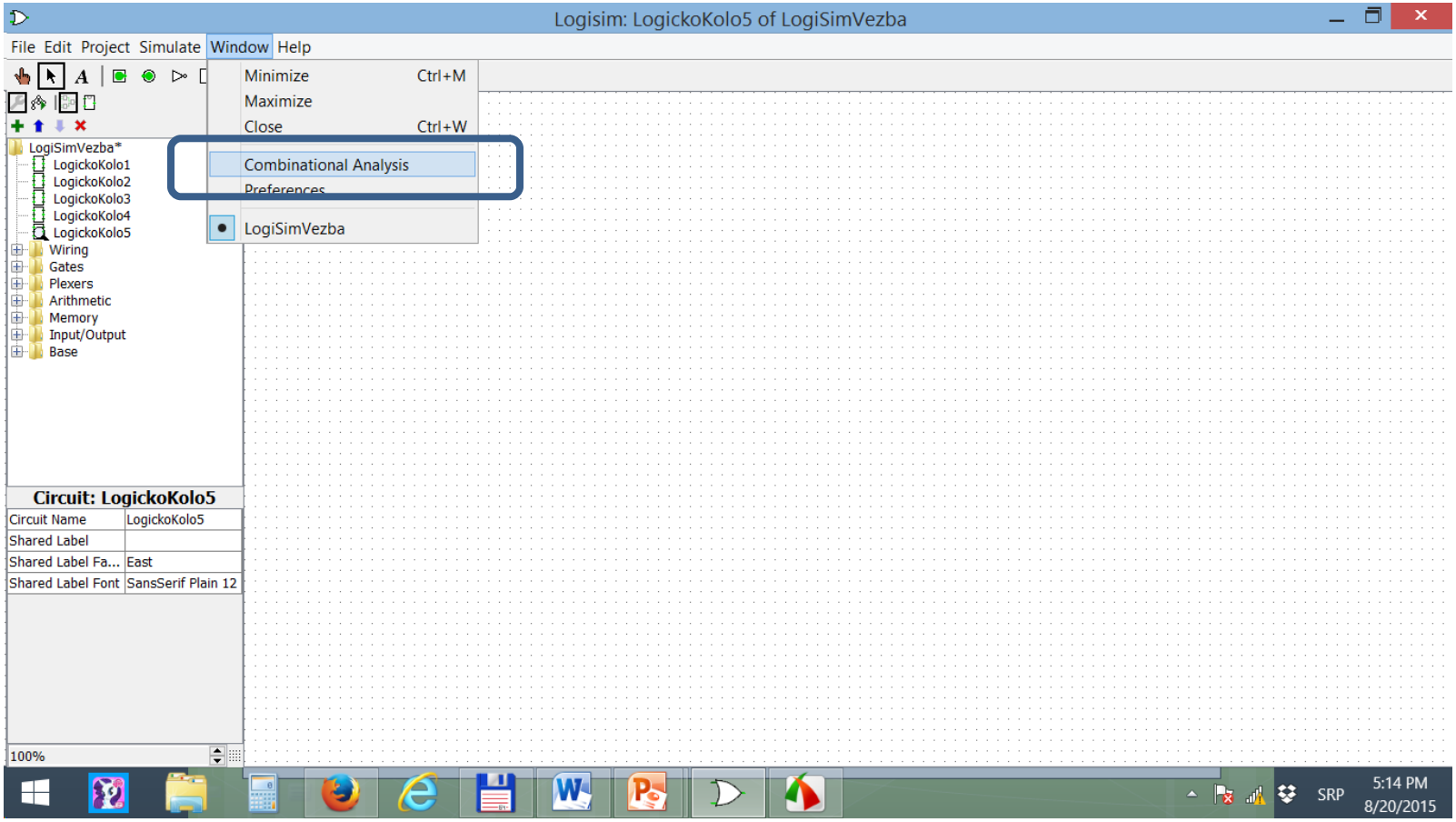
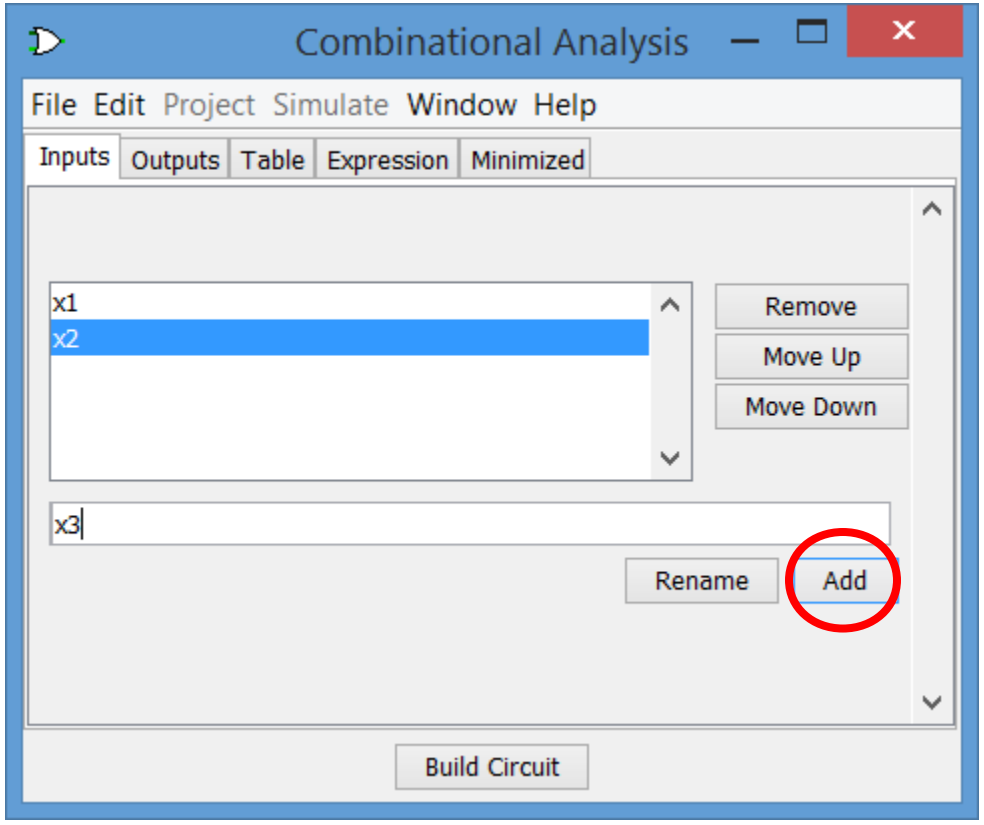
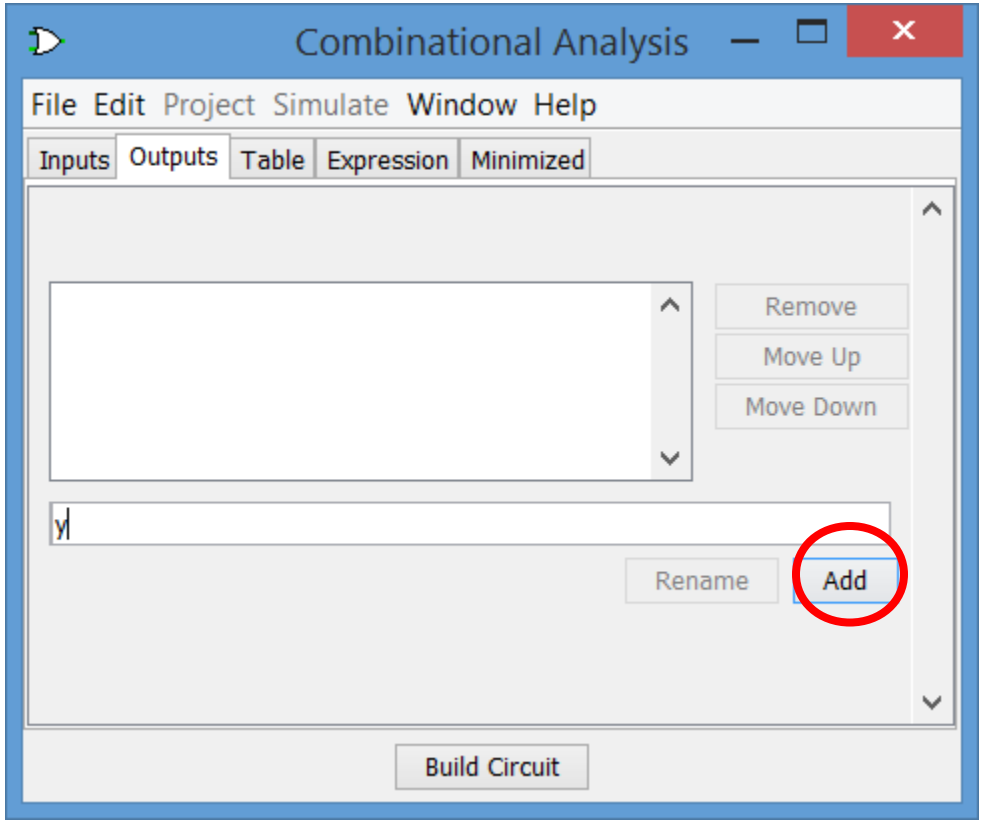
ENG
6:11 PM
8/18/2015


Combinational Analysis
File Edit Project Simulate Window Help
Inputs Outputs Table Expression Minimized
x1 x2 x3 x4 y
0 0 0 0 1
0 0 0 1 0
0 0 1 0 0
0 0 1 1 1
0 1 0 0 0
0 1 0 1 1
0 1 1 0 1
0 1 1 1 0
1 0 0 0 0
1 0 0 1 1
1 0 1 0 1
1 0 1 1 0
1 1 0 0 1
1 1 0 1 0
1 1 1 0 0
1 1 1 1 1
Build Circuit

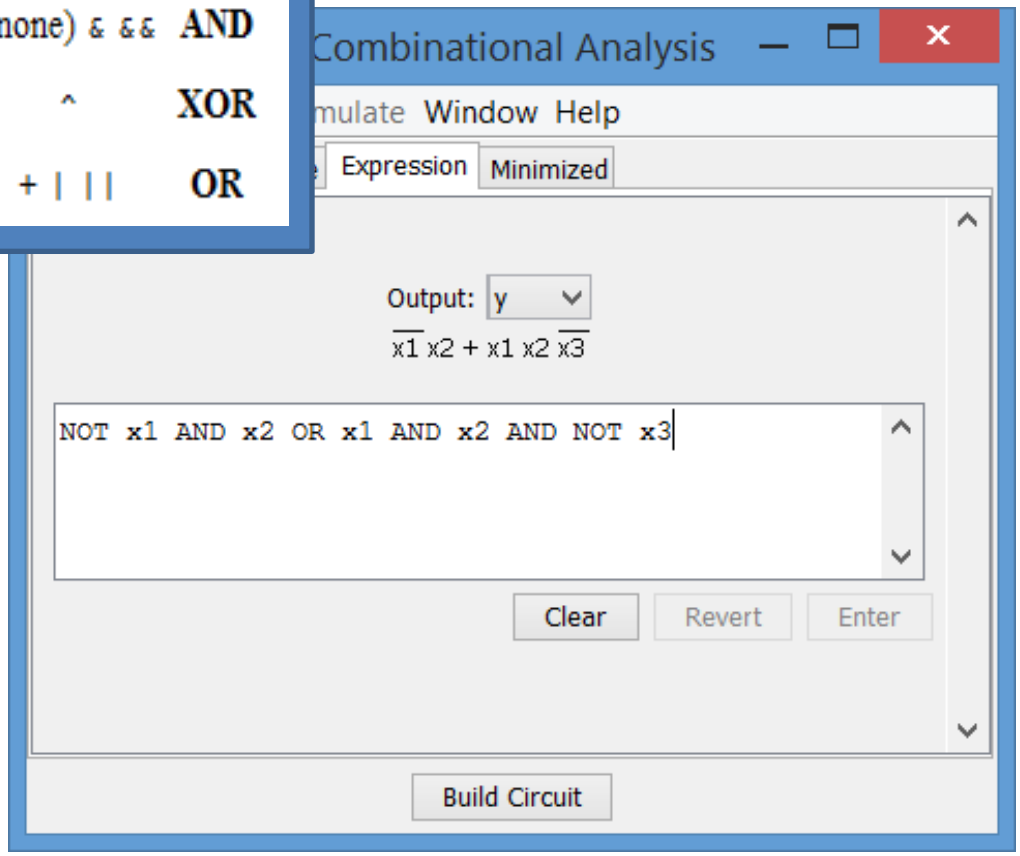

Combinational Analysis
File Edit Project Simulate Window Help
Inputs Outputs Table Expression Minimized
Output: y
Format: Sum of products
x3, x4
00 01 11 10
x1, x2
00 1 0 1 0
01 0 1 0 1
11 1 0 1 0
10 0 1 0 1
x1 x2 x3 x4 + x1 x2 x3 x4
+ x1 x2 x3 x4 + x1 x2 x3 x4
+ x1 x2 x3 x4 + x1 x2 x3 x4
+ x1 x2 x3 x4 + x1 x2 x3 x4
Set As Expression
Build Circuit


Logisim: LogickoKolo5 of LogiSimVezba
File Edit Project Simulate Window Help
Minimize Ctrl+M
Maximize
Close Ctrl+W
Combinational Analysis
Preferences
LogiSimVezba
LogiSimVezba*
LogickoKolo1
LogickoKolo2
LogickoKolo3
LogickoKolo4
LogickoKolo5
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Circuit: LogickoKolo5
Circuit Name LogickoKolo5
Shared Label
Shared Label Fa... East
Shared Label Font SansSerif Plain 12
100%
SRP
5:14 PM
8/20/2015

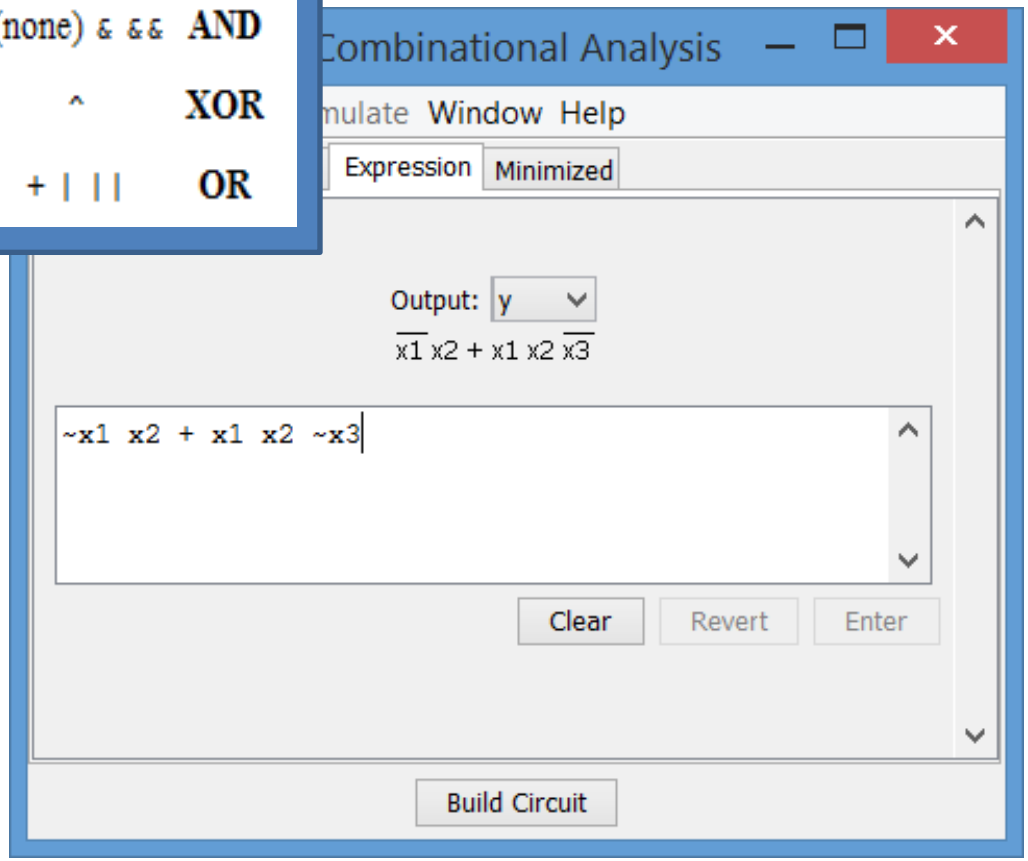

Combinational Analysis
File Edit Project Simulate Window Help
Inputs
Outputs
Table
Expression
Minimized
x1
x2
Remove
Move Up
Move Down
x3
Rename
Add
Build Circuit

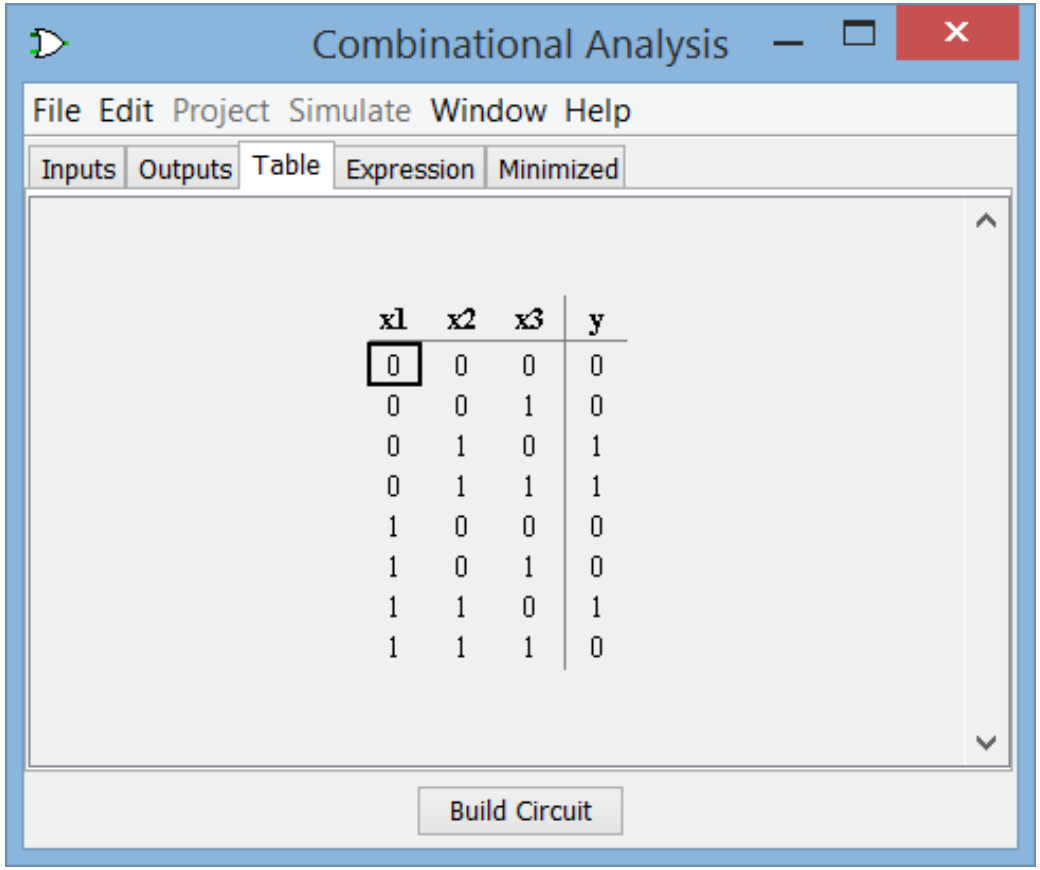

Combinational Analysis
File Edit Project Simulate Window Help
Inputs
Outputs
Table
Expression
Minimized
Remove
Move Up
Move Down
y
Rename
Add
Build Circuit

highest precedence	~ ! '	NOT
	(none) & &&	AND
	^	XOR
lowest precedence	+ | ||	OR

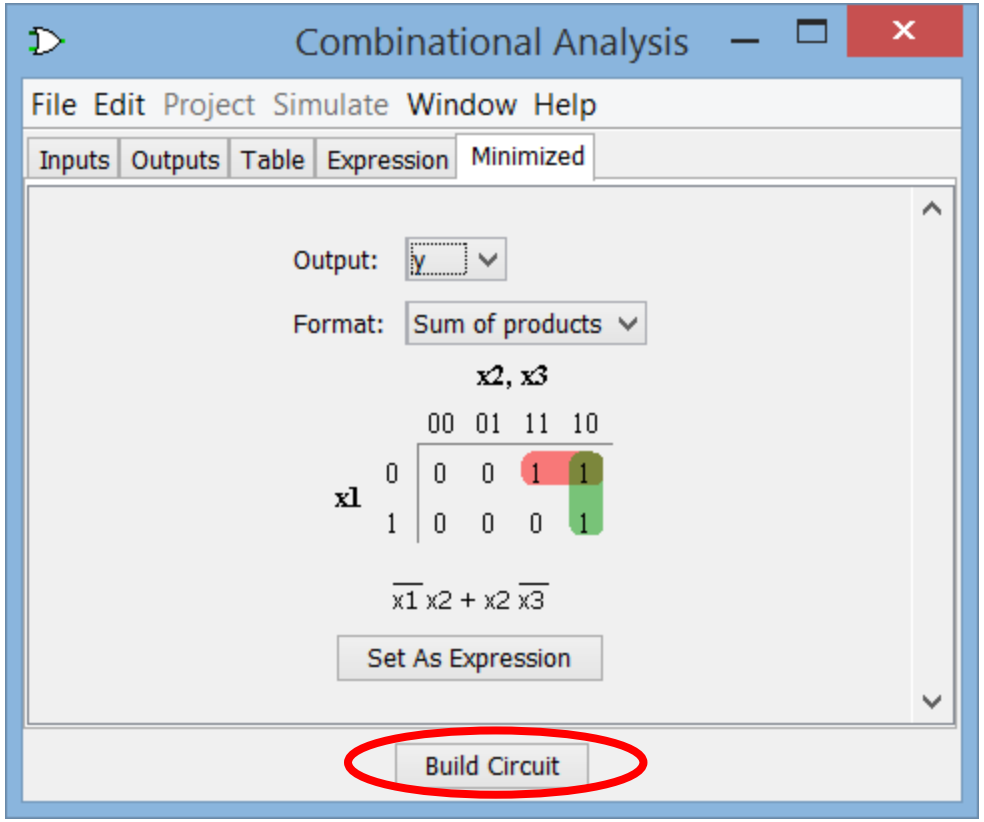


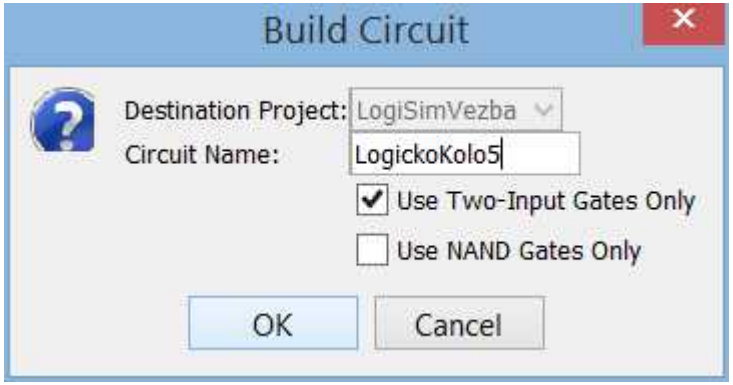
highest precedence	**~ ! '**	**NOT**
	(none) & &&	**AND**
	^	**XOR**
lowest precedence	**+ | ||**	**OR**

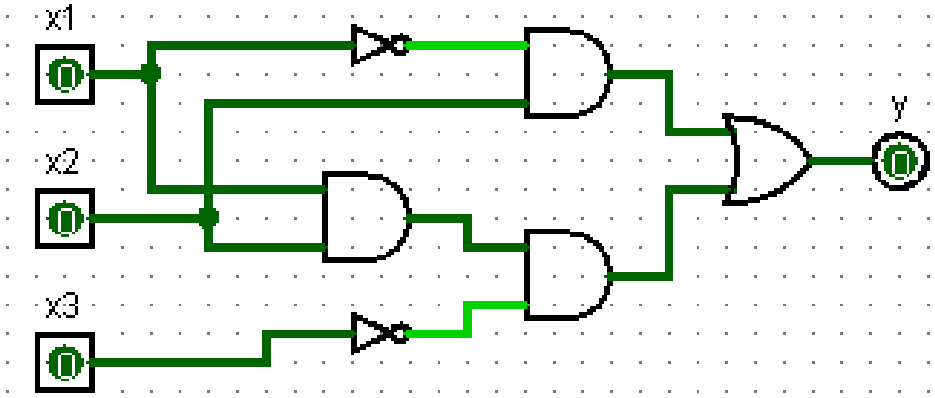


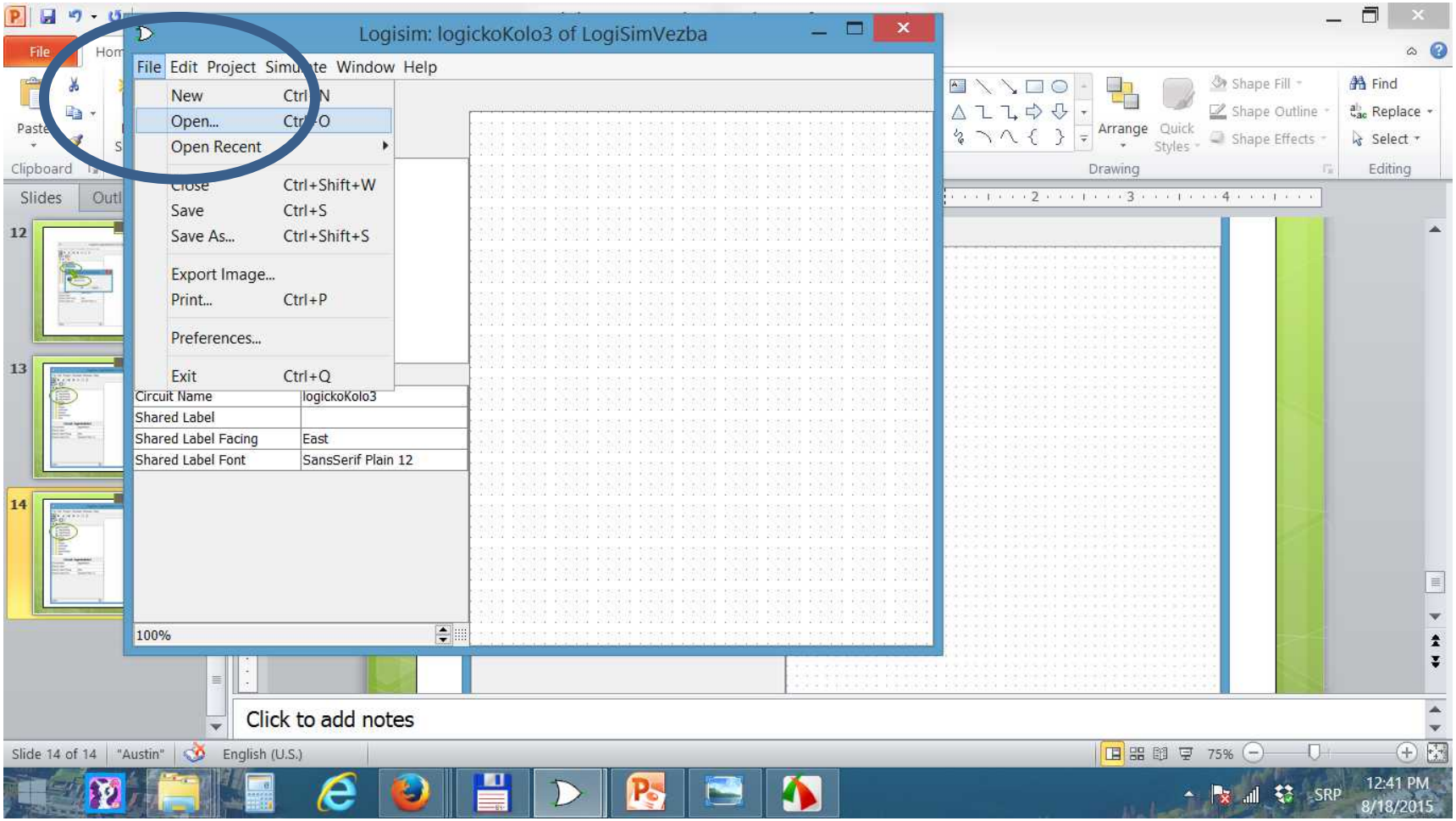

Combinational Analysis
File Edit Project Simulate Window Help
Inputs Outputs Table Expression Minimized
x1 x2 x3 y
0 0 0 0
0 0 1 0
0 1 0 1
0 1 1 1
1 0 0 0
1 0 1 0
1 1 0 1
1 1 1 0
Build Circuit

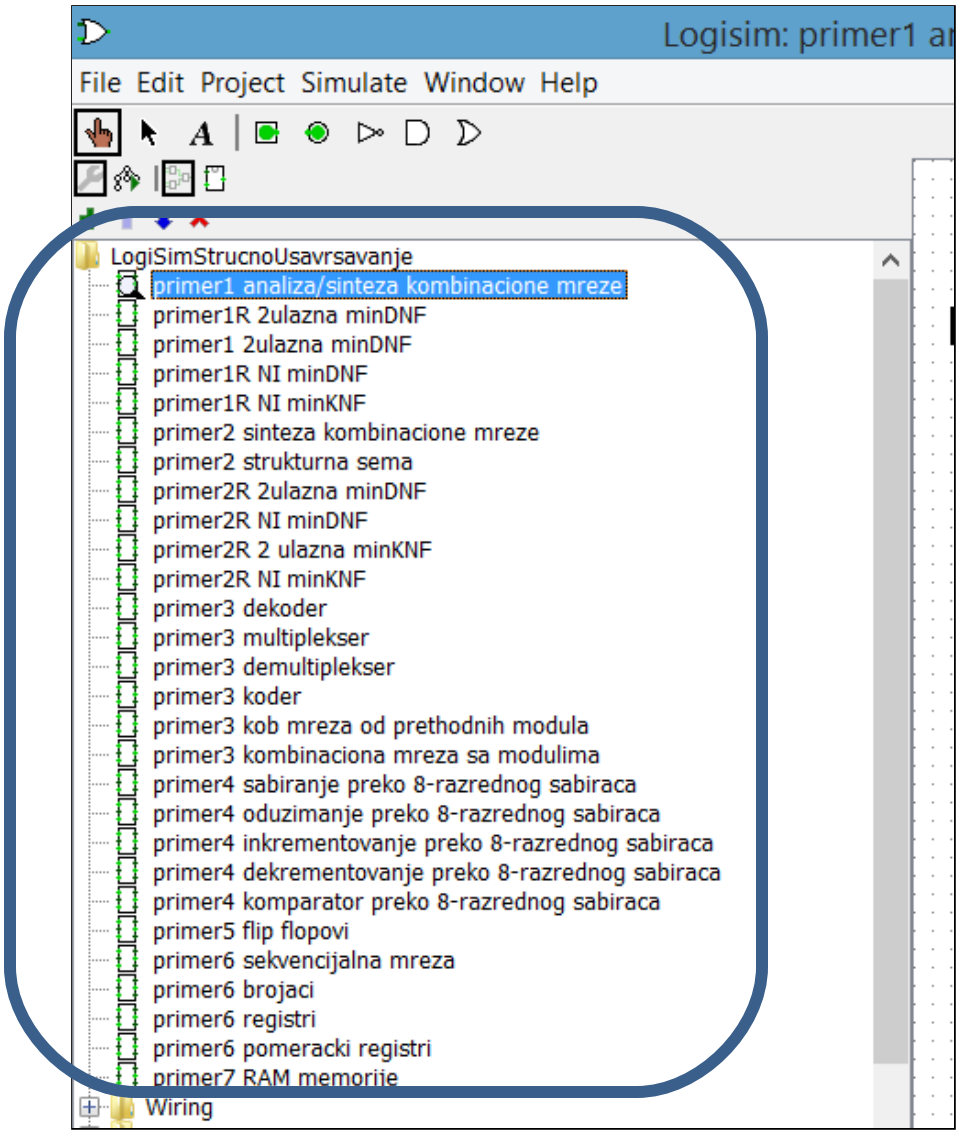
Logisim

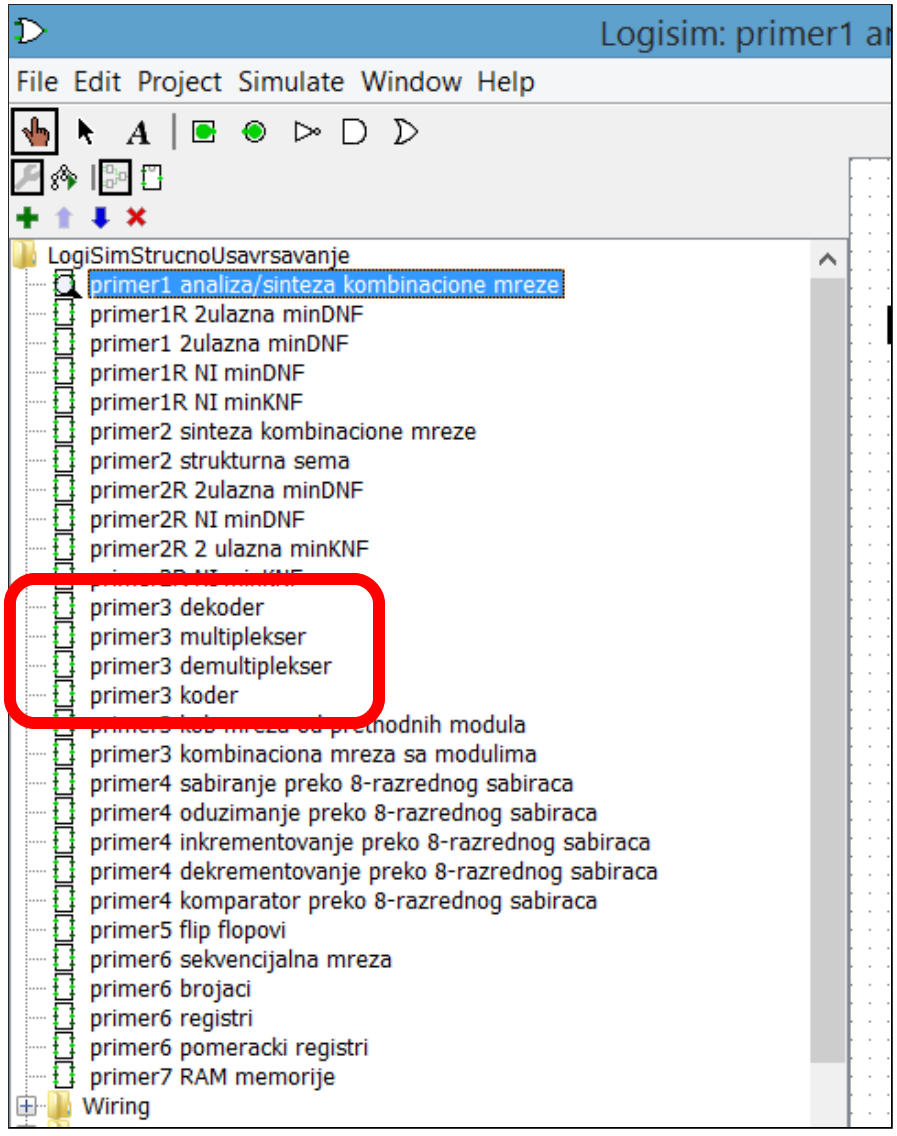

Combinational Analysis
File Edit Project Simulate Window Help
Inputs Outputs Table Expression Minimized
Output: y
Format: Sum of products
x2, x3
00 01 11 10
x1
0 0 0 1 1
1 0 0 0 1
x1 x2 + x2 x3
Set As Expression
Build Circuit

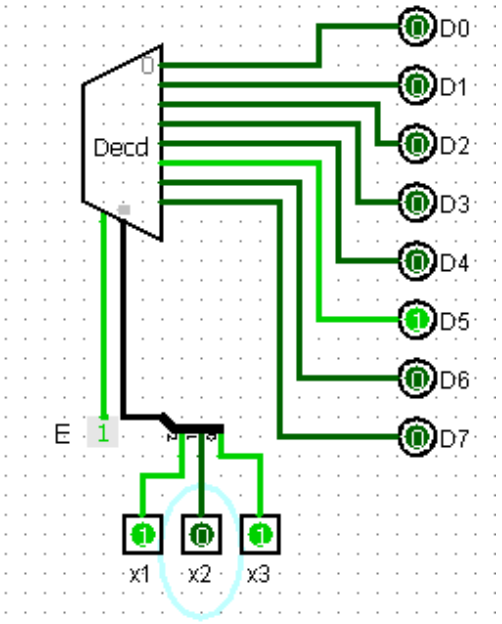

Build Circuit
Destination Project:
LogiSimVezba
Circuit Name:
LogickoKolo5
Use Two-Input Gates Only
Use NAND Gates Only
OK
Cancel

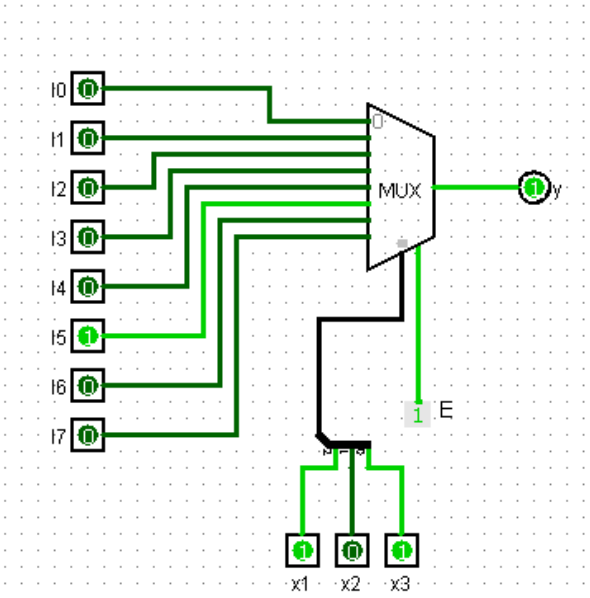

x1
x2
x3
y

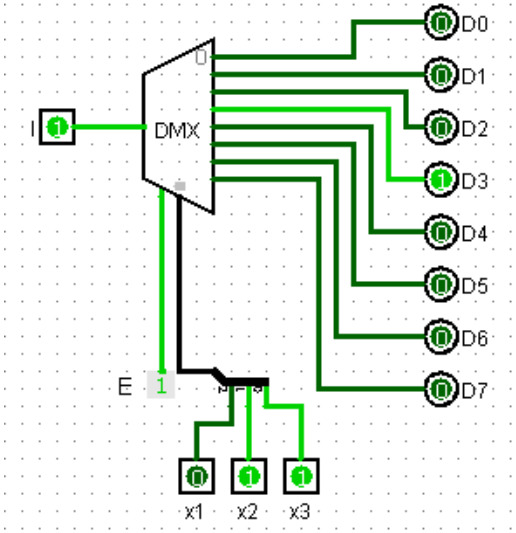

Logisim: logickoKolo3 of LogiSimVezba
File Edit Project Simulate Window Help
New Ctrl+N
Open... Ctrl+O
Open Recent
Close Ctrl+Shift+W
Save Ctrl+S
Save As... Ctrl+Shift+S
Export Image...
Print... Ctrl+P
Preferences...
Exit Ctrl+Q
Circuit Name logickoKolo3
Shared Label
Shared Label Facing East
Shared Label Font SansSerif Plain 12
100%
Click to add notes
Slide 14 of 14
"Austin"
English (U.S.)
75%
SRP
12:41 PM
8/18/2015

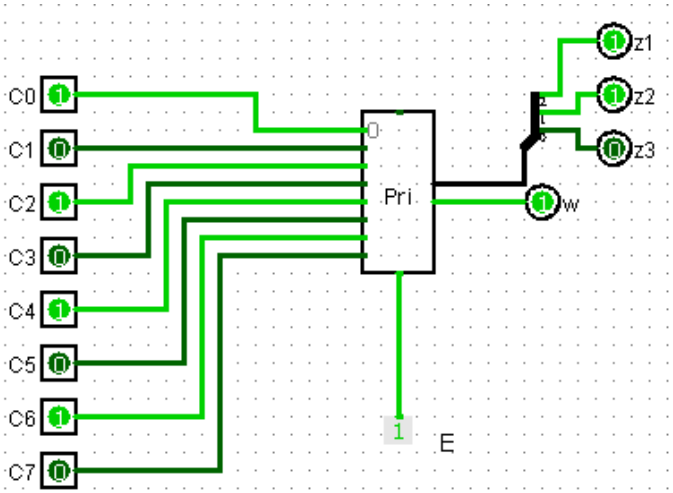

Logisim: primer1 ar
File Edit Project Simulate Window Help
LogiSimStrucnoUsavrsavanje
primer1 analiza/sinteza kombinacione mreze
primer1R 2ulazna minDNF
primer1 2ulazna minDNF
primer1R NI minDNF
primer1R NI minKNF
primer2 sinteza kombinacione mreze
primer2 strukturna sema
primer2R 2ulazna minDNF
primer2R NI minDNF
primer2R 2 ulazna minKNF
primer2R NI minKNF
primer3 dekoder
primer3 multiplekser
primer3 demultiplekser
primer3 koder
primer3 kob mreza od prethodnih modula
primer3 kombinaciona mreza sa modulima
primer4 sabiranje preko 8-razrednog sabiraca
primer4 oduzimanje preko 8-razrednog sabiraca
primer4 inkrementovanje preko 8-razrednog sabiraca
primer4 dekrementovanje preko 8-razrednog sabiraca
primer4 komparator preko 8-razrednog sabiraca
primer5 flip flopovi
primer6 sekvencijalna mreza
primer6 brojaci
primer6 registri
primer6 pomeracki registri
primer7 RAM memorije
Wiring

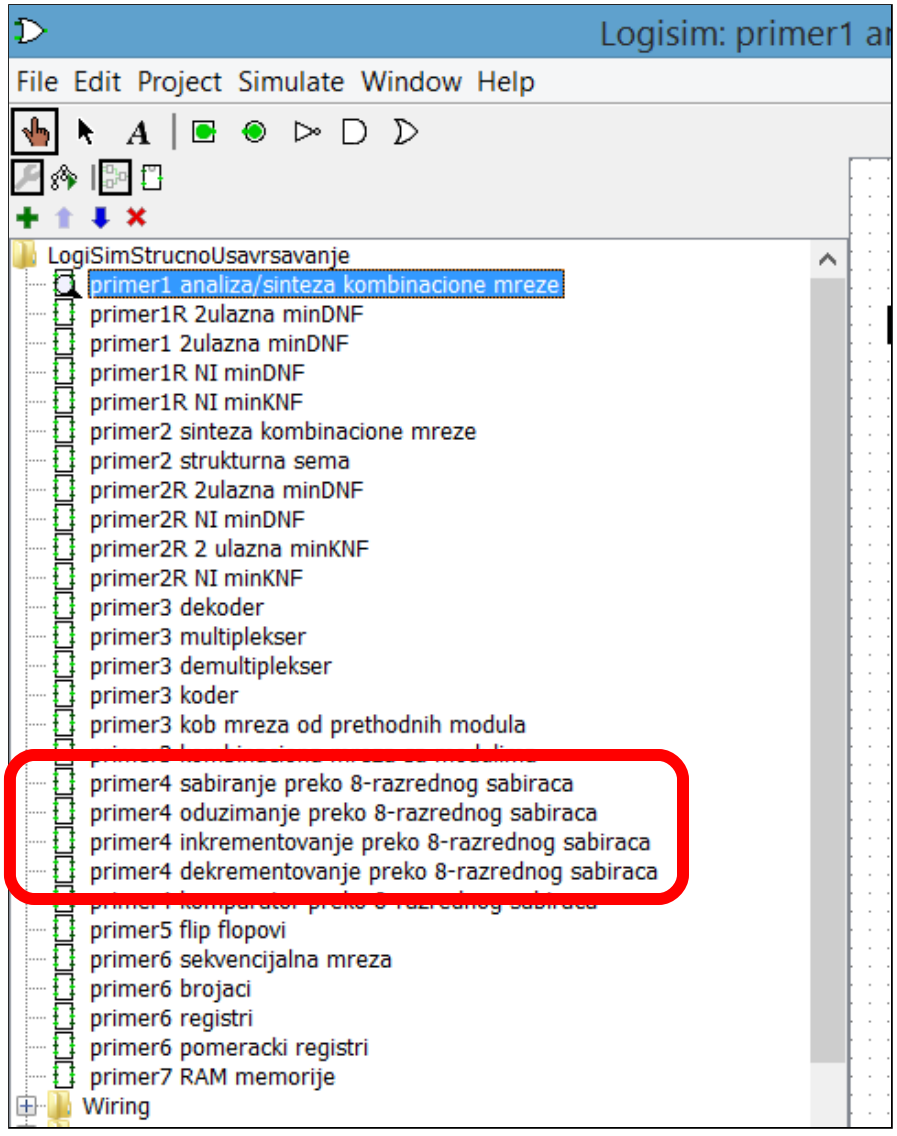

Logisim: primer1 ar
File Edit Project Simulate Window Help
LogiSimStrucnoUsavrsavanje
primer1 analiza/sinteza kombinacione mreze
primer1R 2ulazna minDNF
primer1 2ulazna minDNF
primer1R NI minDNF
primer1R NI minKNF
primer2 sinteza kombinacione mreze
primer2 strukturna sema
primer2R 2ulazna minDNF
primer2R NI minDNF
primer2R 2 ulazna minKNF
primer3 dekoder
primer3 multiplekser
primer3 demultiplekser
primer3 koder
primer3 kombinaciona mreza sa modulima
primer4 sabiranje preko 8-razrednog sabiraca
primer4 oduzimanje preko 8-razrednog sabiraca
primer4 inkrementovanje preko 8-razrednog sabiraca
primer4 dekrementovanje preko 8-razrednog sabiraca
primer4 komparator preko 8-razrednog sabiraca
primer5 flip flopovi
primer6 sekvencijalna mreza
primer6 brojaci
primer6 registri
primer6 pomeracki registri
primer7 RAM memorije
Wiring

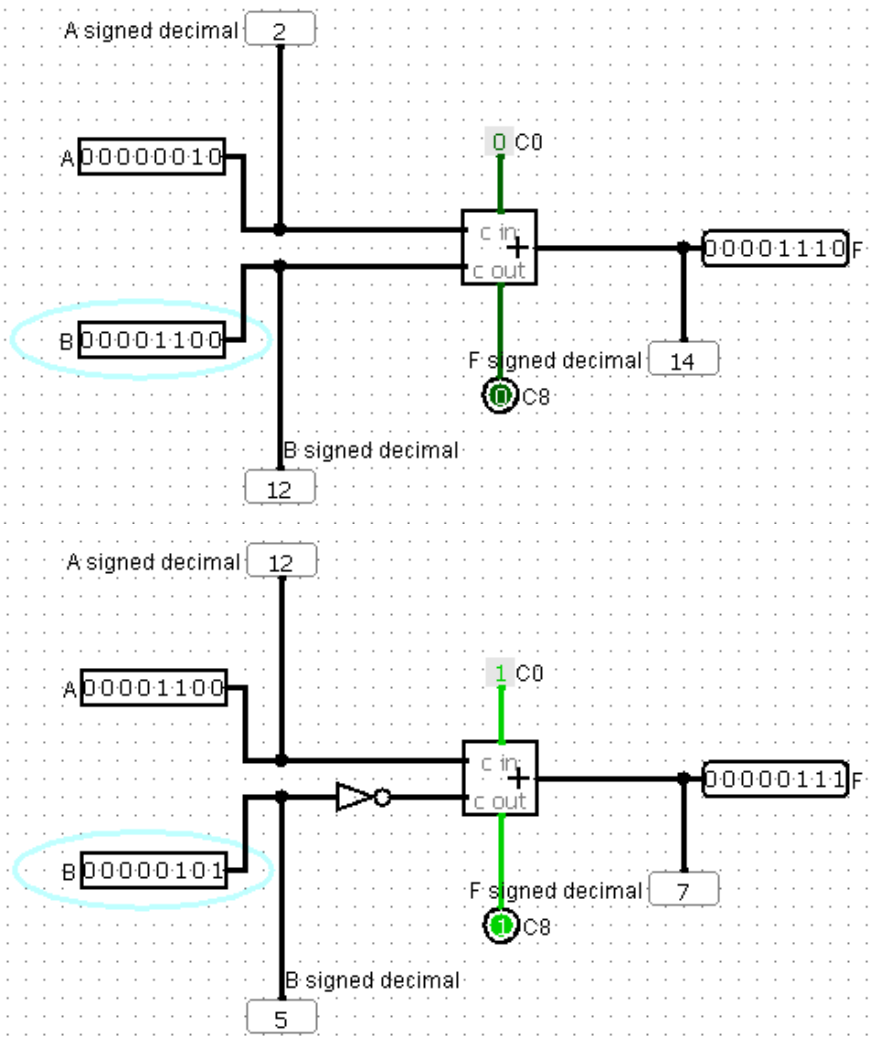

Decd
D0
D1
D2
D3
D4
D5
D6
D7
E
1
x1
x2
x3


MUX
I0
I1
I2
I3
I4
I5
I6
I7
y
1
E
x1
x2
x3

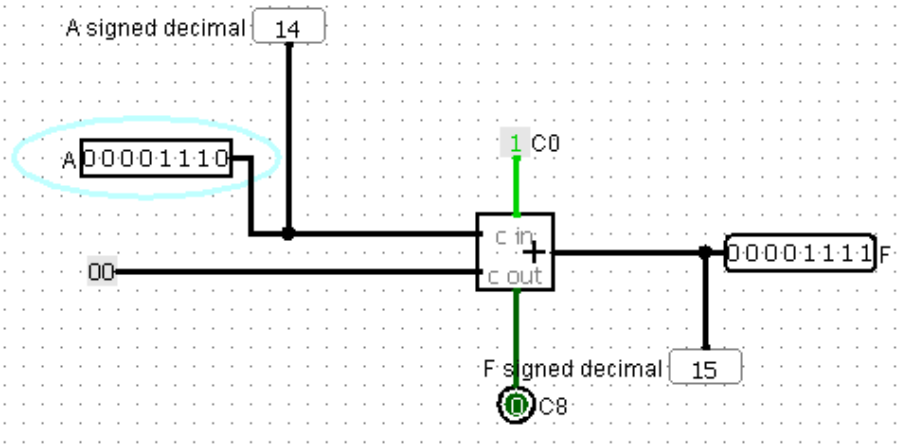

DMX
I
D0
D1
D2
D3
D4
D5
D6
D7
E
1
x1
x2
x3

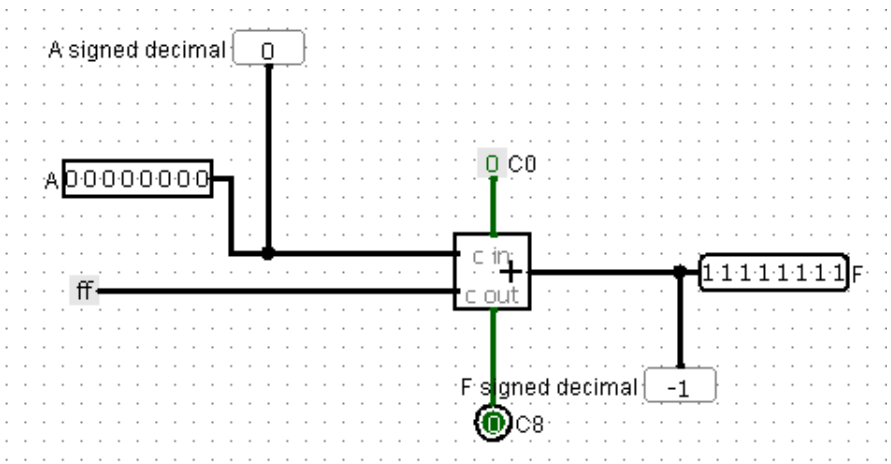

Pri
C0
C1
C2
C3
C4
C5
C6
C7
z1
z2
z3
w
1
E


Logisim: primer1 ar
File Edit Project Simulate Window Help
LogiSimStrucnoUsavrsavanje
primer1 analiza/sinteza kombinacione mreze
primer1R 2ulazna minDNF
primer1 2ulazna minDNF
primer1R NI minDNF
primer1R NI minKNF
primer2 sinteza kombinacione mreze
primer2 strukturna sema
primer2R 2ulazna minDNF
primer2R NI minDNF
primer2R 2 ulazna minKNF
primer2R NI minKNF
primer3 dekoder
primer3 multiplekser
primer3 demultiplekser
primer3 koder
primer3 kob mreza od prethodnih modula
primer4 sabiranje preko 8-razrednog sabiraca
primer4 oduzimanje preko 8-razrednog sabiraca
primer4 inkrementovanje preko 8-razrednog sabiraca
primer4 dekrementovanje preko 8-razrednog sabiraca
primer5 flip flopovi
primer6 sekvencijalna mreza
primer6 brojaci
primer6 registri
primer6 pomeracki registri
primer7 RAM memorije
Wiring

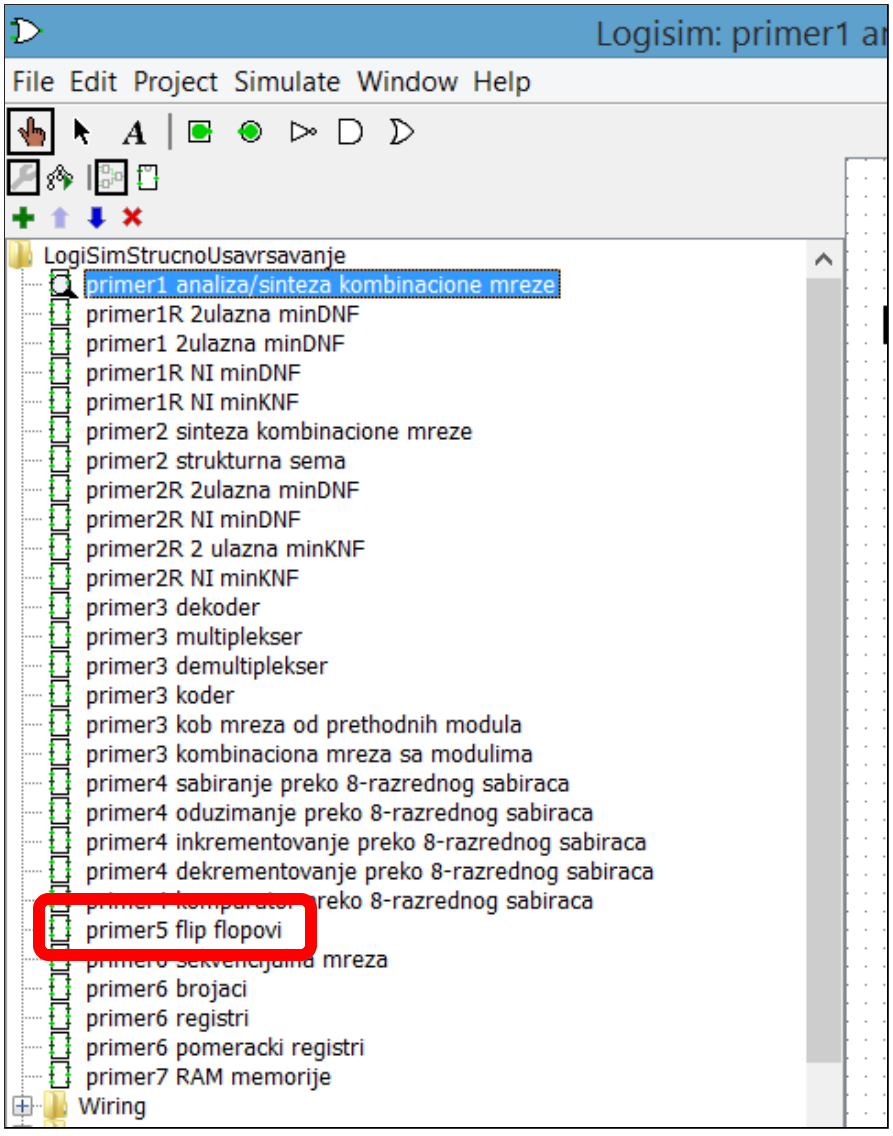


$$F = A - B = A + (-B) = A + \overline{(-B)}^{2} = A + \overline{B} + 1$$





$$F = A - 1 = A + (-1) = A + \overline{(-1)}^{2} = A + \overline{00000001} + 1 = A + 11111110 + 1 = A + 11111111$$


Logisim: primer1 ar
File Edit Project Simulate Window Help
LogiSimStrucnoUsavrsavanje
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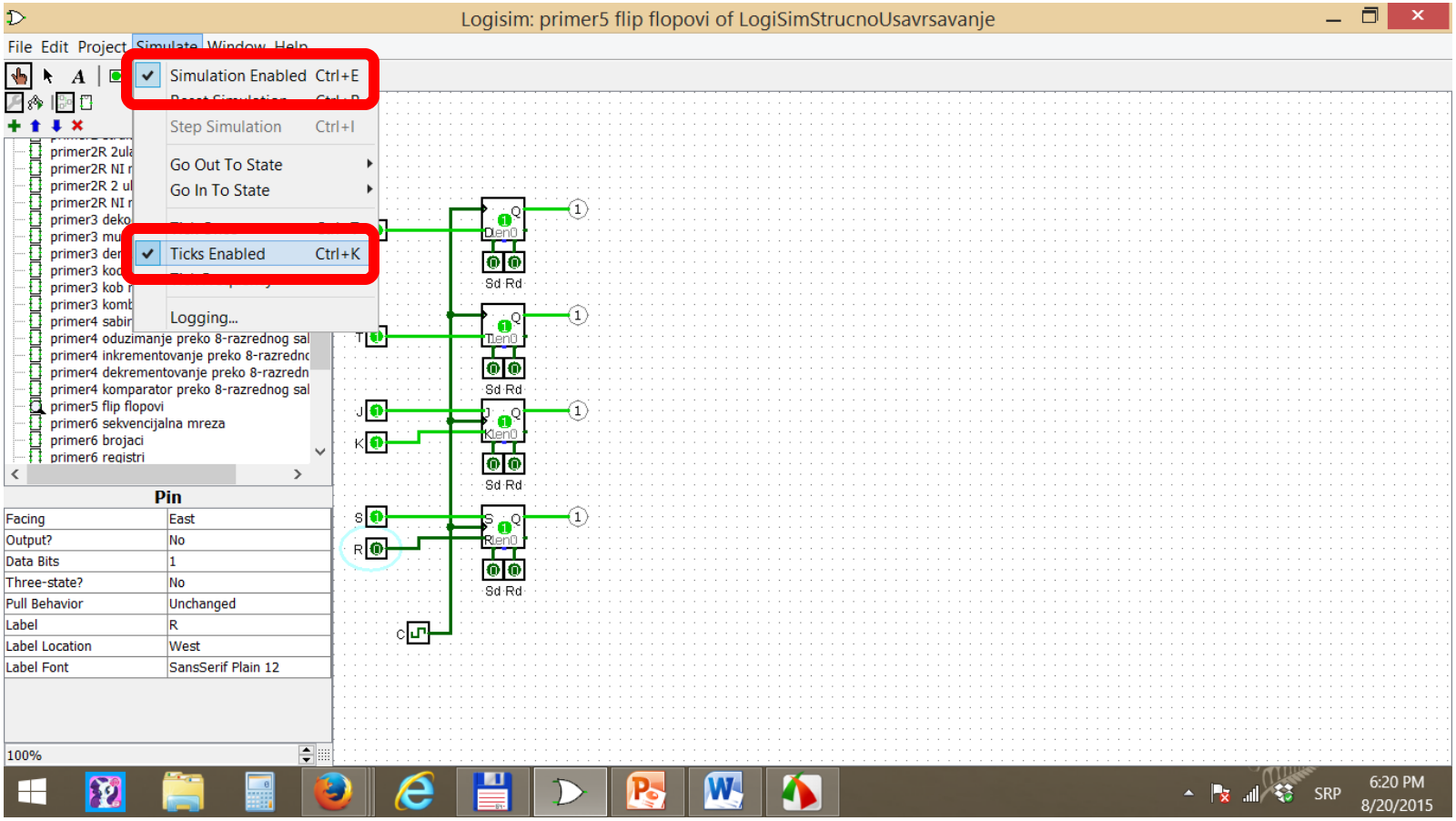
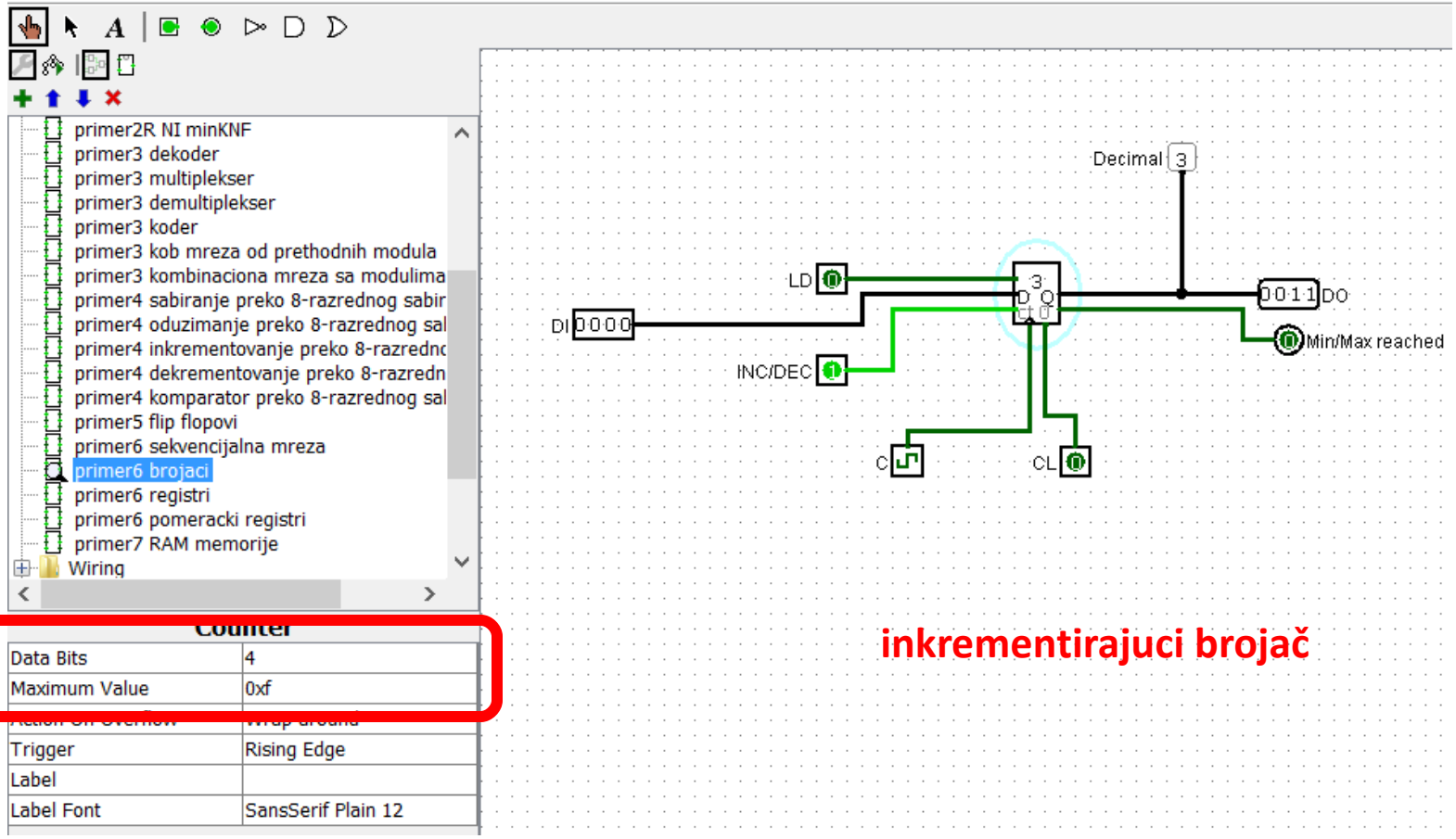
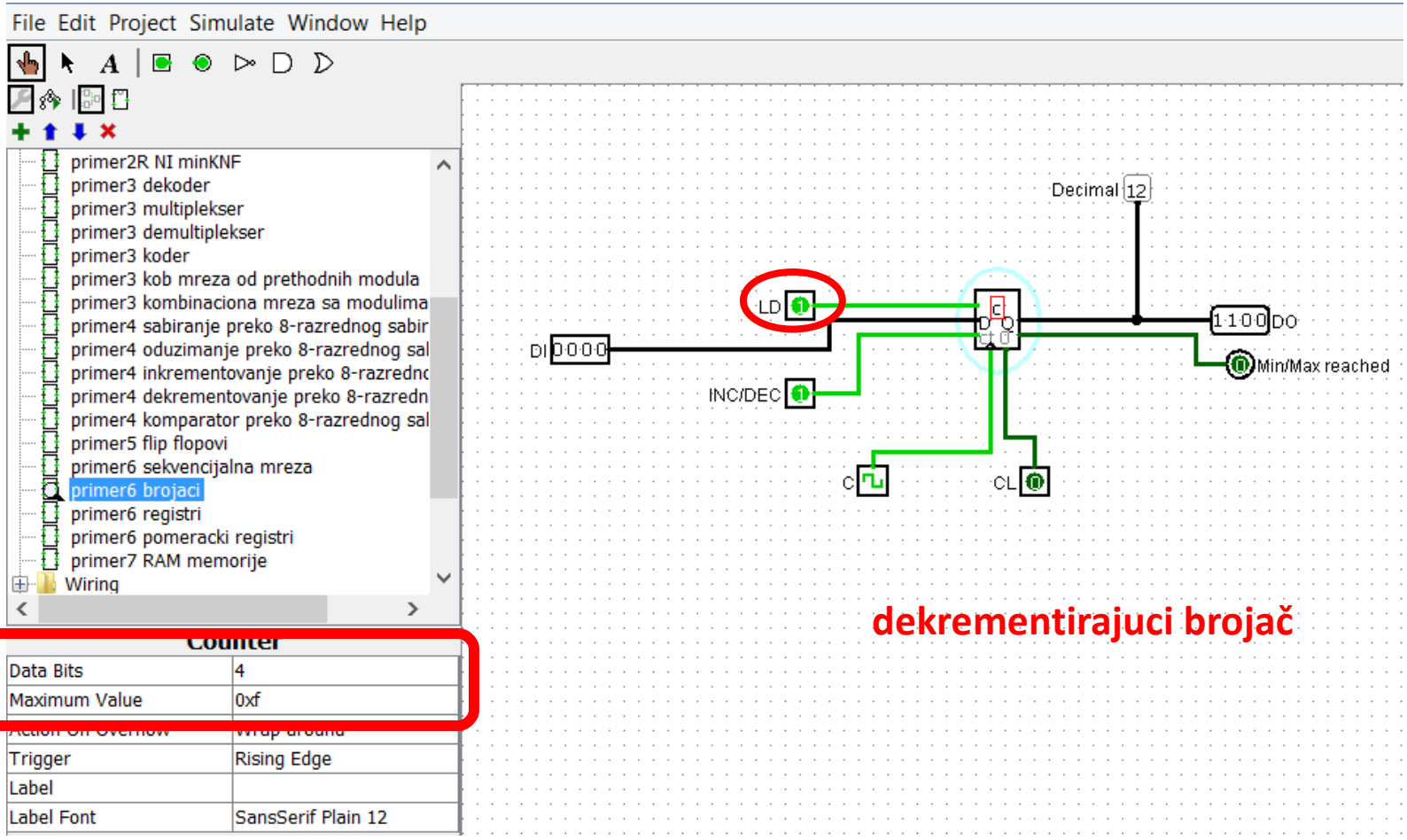
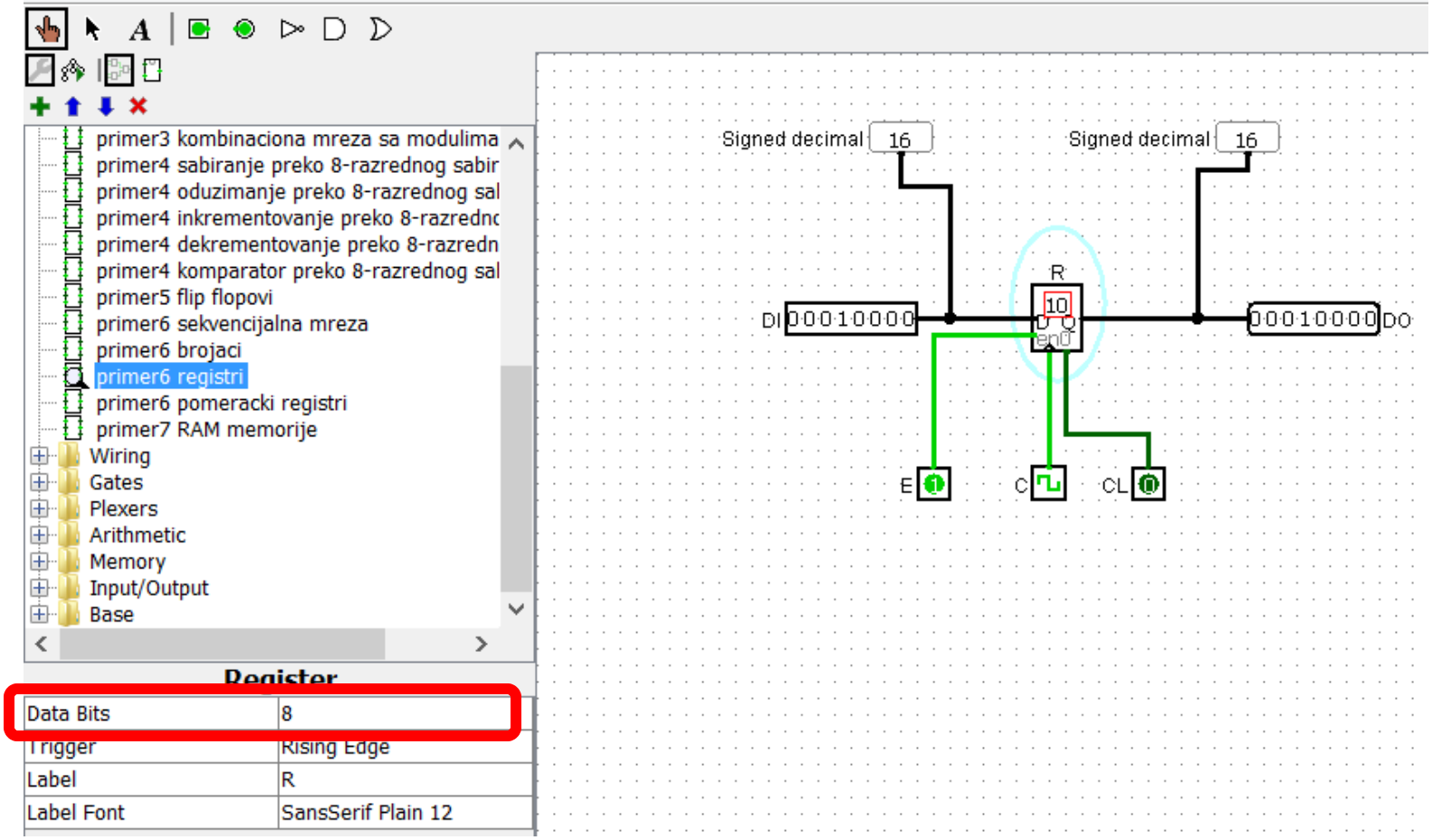
primer1R 2ulazna minDNF
primer1 2ulazna minDNF
primer1R NI minDNF
primer1R NI minKNF
primer2 sinteza kombinacione mreze
primer2 strukturna sema
primer2R 2ulazna minDNF
primer2R NI minDNF
primer2R 2 ulazna minKNF
primer2R NI minKNF
primer3 dekoder
primer3 multiplekser
primer3 demultiplekser
primer3 koder
primer3 kob mreza od prethodnih modula
primer3 kombinaciona mreza sa modulima
primer4 sabiranje preko 8-razrednog sabiraca
primer4 oduzimanje preko 8-razrednog sabiraca
primer4 inkrementovanje preko 8-razrednog sabiraca
primer4 dekrementovanje preko 8-razrednog sabiraca
reko 8-razrednog sabiraca
primer5 flip flopovi
mreza
primer6 brojaci
primer6 registri
primer6 pomeracki registri
primer7 RAM memorije
Wiring


Logisim: primer5 flip flopovi of LogiSimStrucnoUsavrsavanje
File Edit Project Simulate Window Help
Simulation Enabled Ctrl+E
Step Simulation Ctrl+I
Go Out To State
Go In To State
Ticks Enabled Ctrl+K
Logging...
primer4 komparator preko 8-razrednog sal
primer5 flip flopovi
primer6 sekvencijalna mreza
primer6 brojaci
primer6 registri
Pin
Facing East
Output? No
Data Bits 1
Three-state? No
Pull Behavior Unchanged
Label R
Label Location West
Label Font SansSerif Plain 12
100%
T
J
K
S
R
C
Sd Rd
SRP
6:20 PM
8/20/2015



inkrementirajuci brojač


File Edit Project Simulate Window Help
primer2R NI minKNF
primer3 dekoder
primer3 multiplekser
primer3 demultiplekser
primer3 koder
primer3 kob mreza od prethodnih modula
primer3 kombinaciona mreza sa modulima
primer4 sabiranje preko 8-razrednog sabir
primer4 oduzimanje preko 8-razrednog sal
primer4 inkrementovanje preko 8-razredn
primer4 dekrementovanje preko 8-razredn
primer4 komparator preko 8-razrednog sal
primer5 flip flopovi
primer6 sekvencijalna mreza
primer6 brojaci
primer6 registri
primer6 pomeracki registri
primer7 RAM memorije
Wiring
Counter
Data Bits 4
Maximum Value 0xf
Trigger Rising Edge
Label
Label Font SansSerif Plain 12
Decimal 12
LD
DI 0000
INC/DEC
C
CL
1100 DO
Min/Max reached
dekrementirajuci brojač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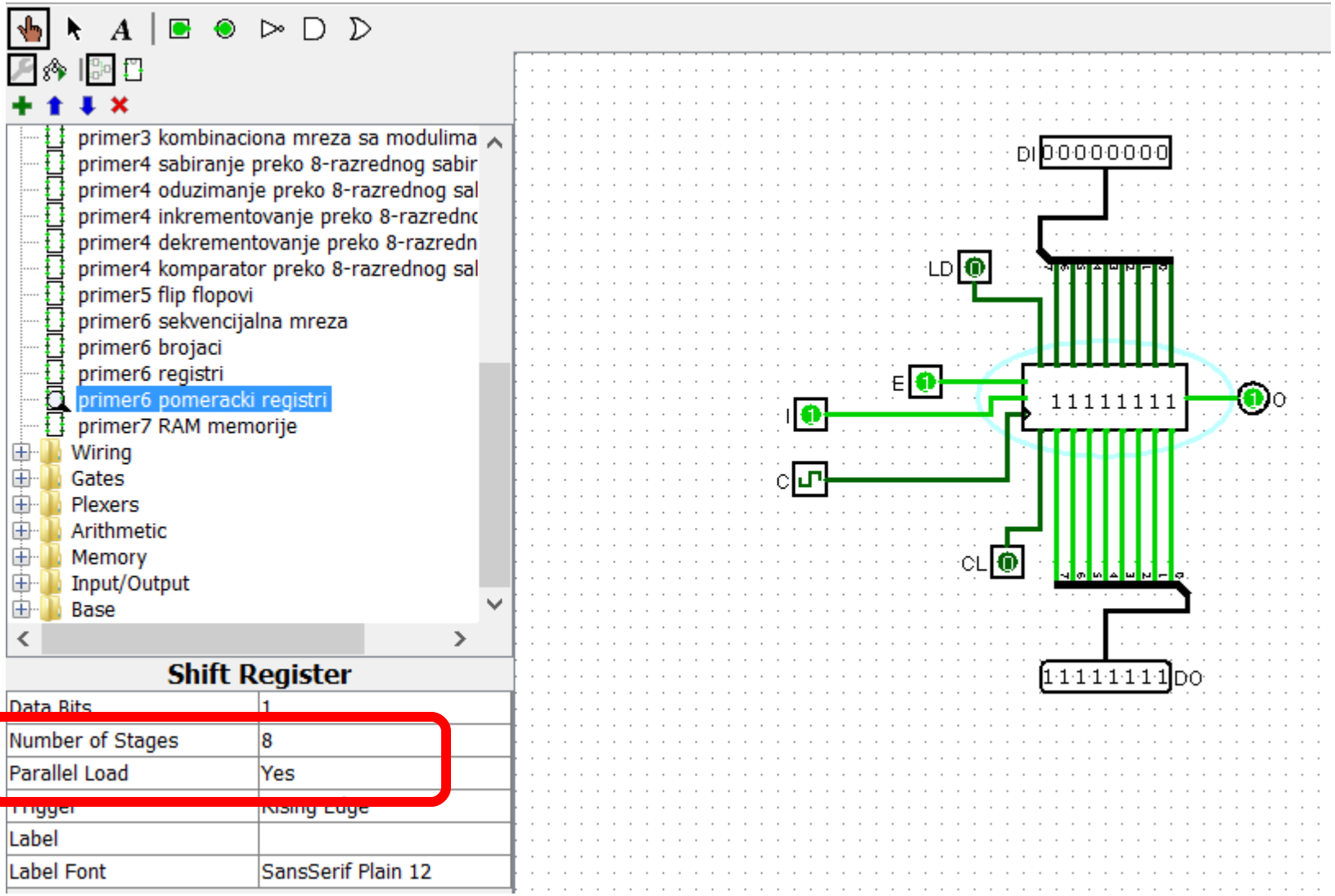
primer4 sabiranje preko 8-razrednog sabir
primer4 oduzimanje preko 8-razrednog sal
primer4 inkrementovanje preko 8-razrednc
primer4 dekrementovanje preko 8-razredn
primer4 komparator preko 8-razrednog sal
primer5 flip flopovi
primer6 sekvencijalna mreza
primer6 brojaci
primer6 registri
primer6 pomeracki registri
primer7 RAM memorije
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Register
Data Bits 8
Trigger Rising Edge
Label R
Label Font SansSerif Plain 12
Signed decimal 16
Signed decimal 16
R
10
DI 00010000
00010000 DO
E
C
CL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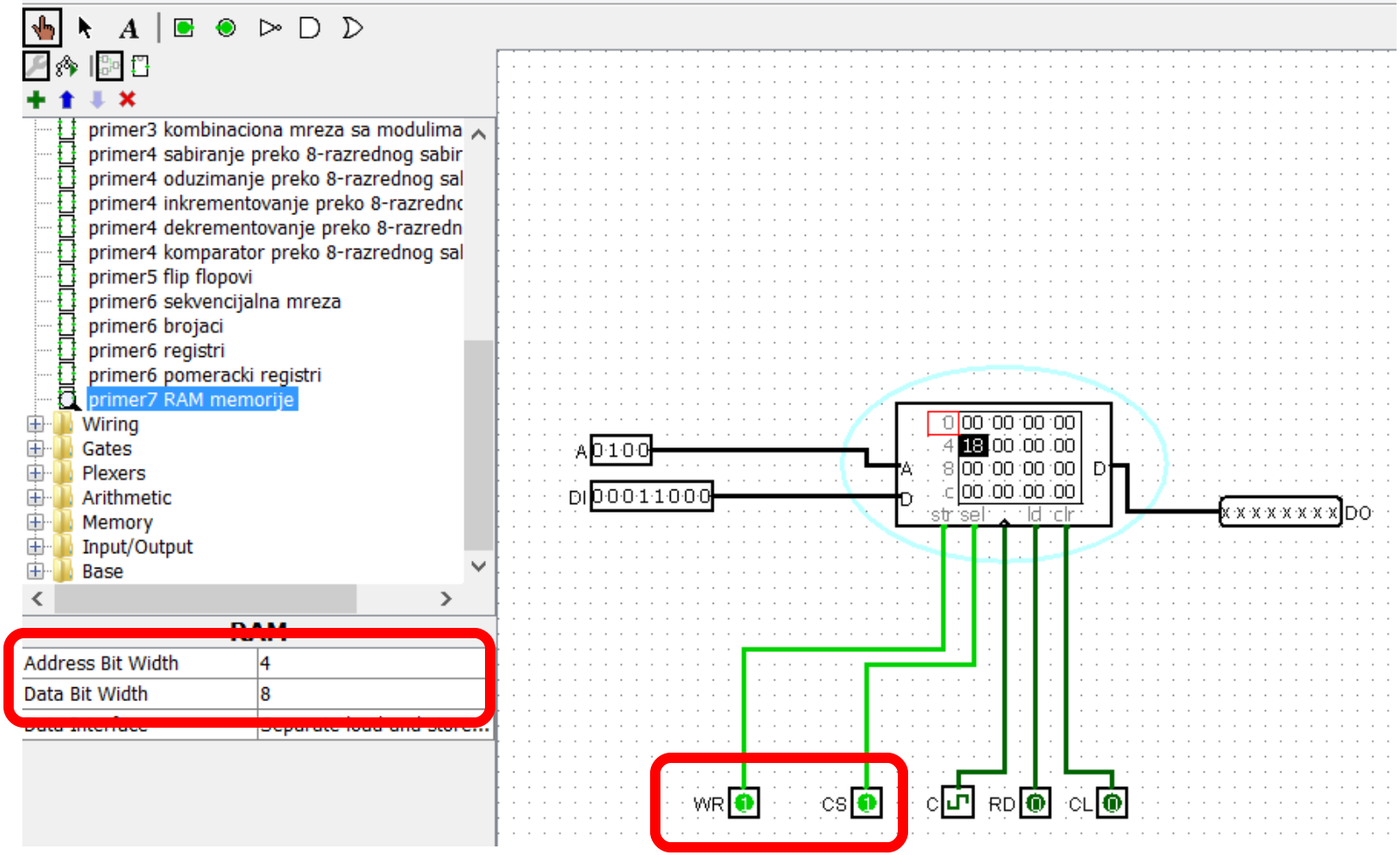
primer4 dekrementovanje preko 8-razredn
primer4 komparator preko 8-razrednog sal
primer5 flip flopovi
primer6 sekvencijalna mreza
primer6 brojaci
primer6 registri
primer6 pomeracki registri
primer7 RAM memorije
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Shift Register
Data Bits 1
Number of Stages 8
Parallel Load Yes
Label
Label Font SansSerif Plain 12
DI 00000000
LD
E
I
C
CL
11111111
O
11111111 DO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primer4 oduzimanje preko 8-razrednog sal
primer4 inkrementovanje preko 8-razrednc
primer4 dekrementovanje preko 8-razredn
primer4 komparator preko 8-razrednog sal
primer5 flip flopovi
primer6 sekvencijalna mreza
primer6 brojaci
primer6 registri
primer6 pomeracki registri
primer7 RAM memorije
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
RAM
Address Bit Width
4
Data Bit Width
8
A
0100
DI
00011000
A
D
0 00 00 00 00
4 18 00 00 00
8 00 00 00 00
c 00 00 00 00
str sel ld clr
D
xxxxxxxx
DO
WR
CS
C
RD
CL