

Polusabirac

Polusabirac

New Project Wizard

Create New Project

Specify project location and type.

Enter a name, locations, and comment for the project

Name: Polusabirac

Location: E:\fakultet\Fin\ORT_2\nedelje\Nedelja_2\Polusabirac

Working Directory: E:\fakultet\Fin\ORT_2\nedelje\Nedelja_2\Polusabirac

Description:

Select the type of top-level source for the project

Top-level source type: HDL

More Info Next Cancel

Polusabirac

New Project Wizard

Project Settings

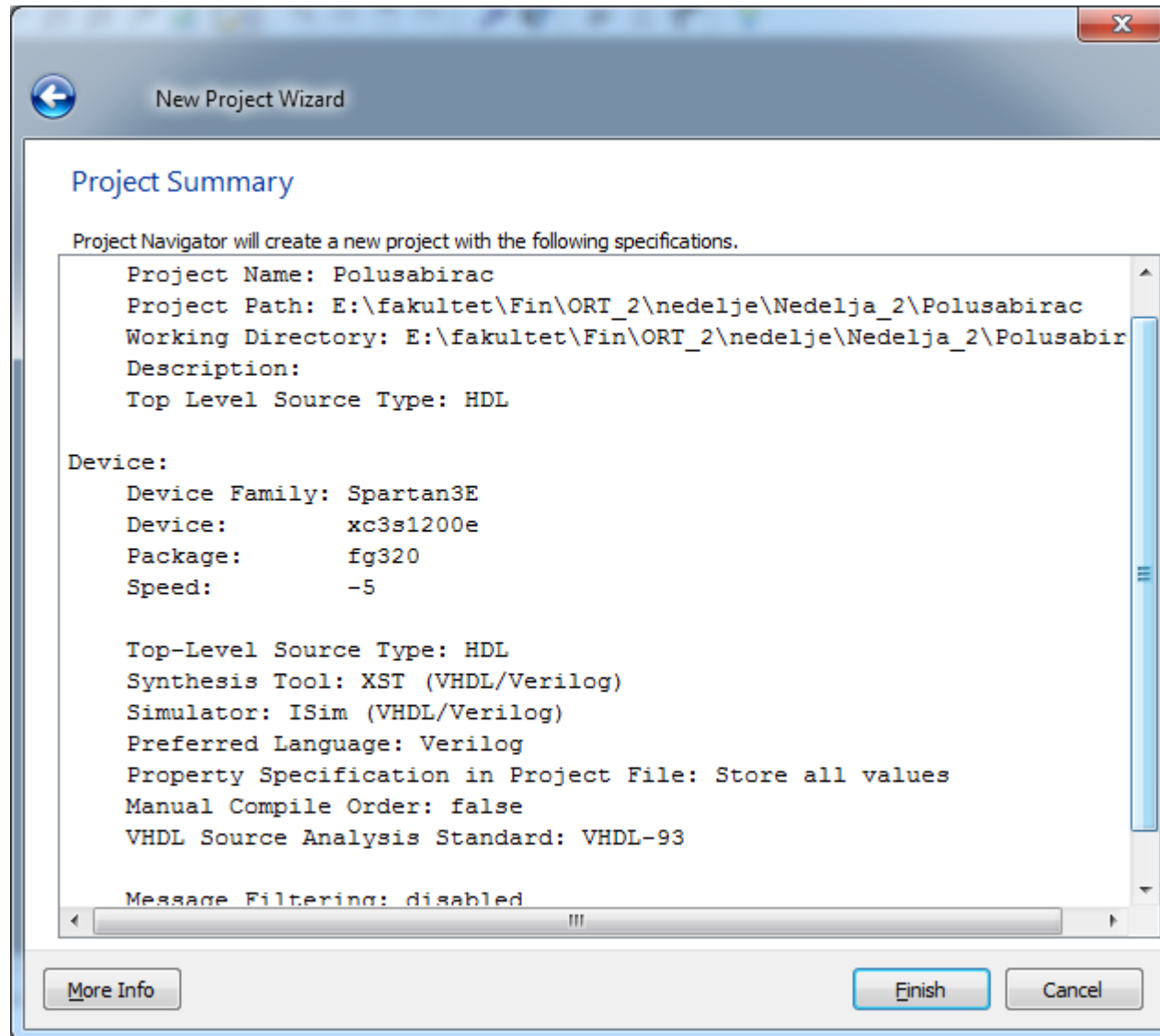
Specify device and project properties.
Select the device and design flow for the project

Property Name	Value
Evaluation Development Board	None Specified
Product Category	All
Family	Spartan3E
Device	XC3S1200E
Package	FG320
Speed	-5
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	Verilog
Property Specification in Project File	Store all values
Manual Compile Order	<input type="checkbox"/>
VHDL Source Analysis Standard	VHDL-93
Enable Message Filtering	<input type="checkbox"/>

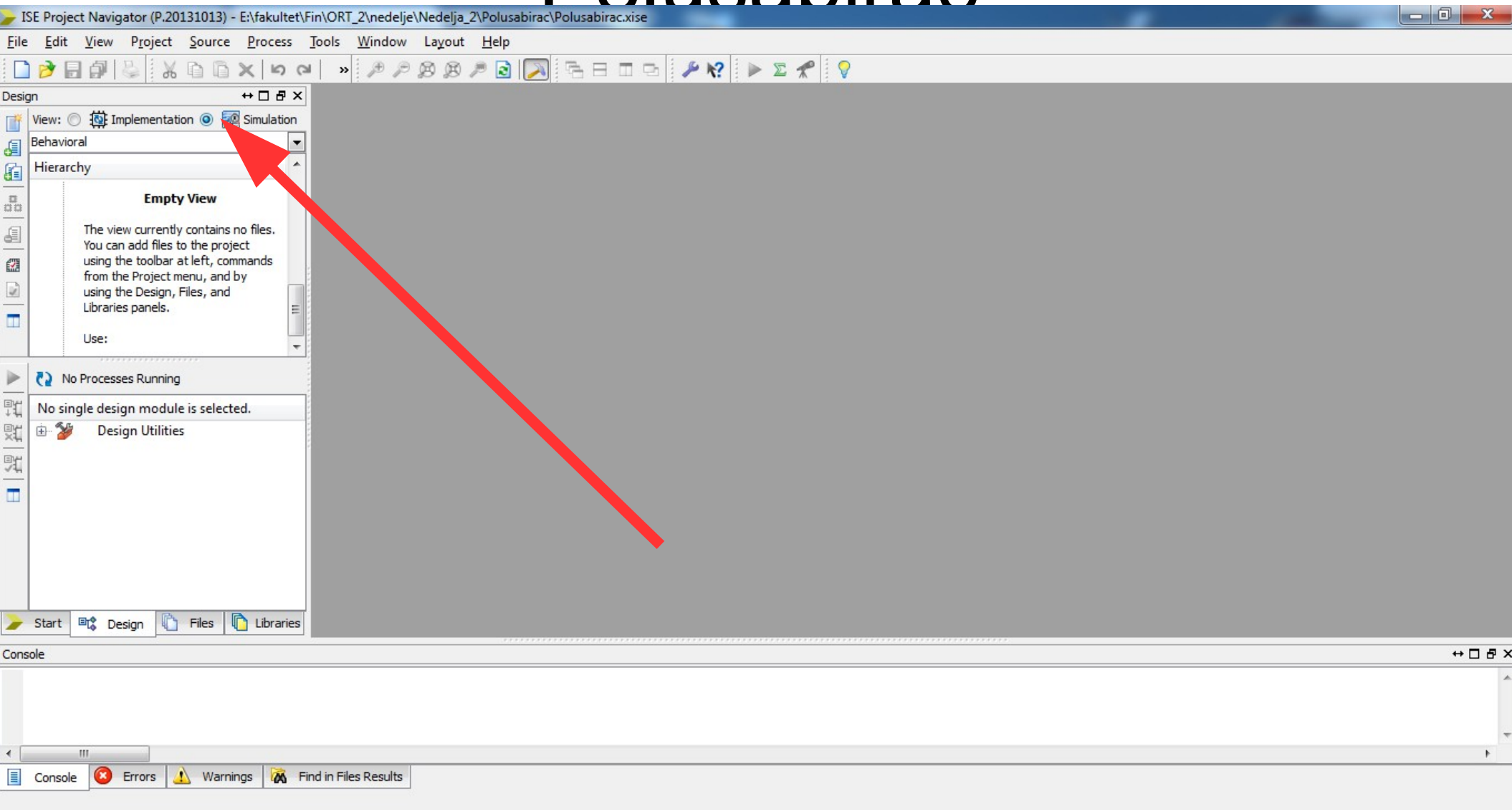
Default: ISim (VHDL/Verilog)

More Info Next Cancel

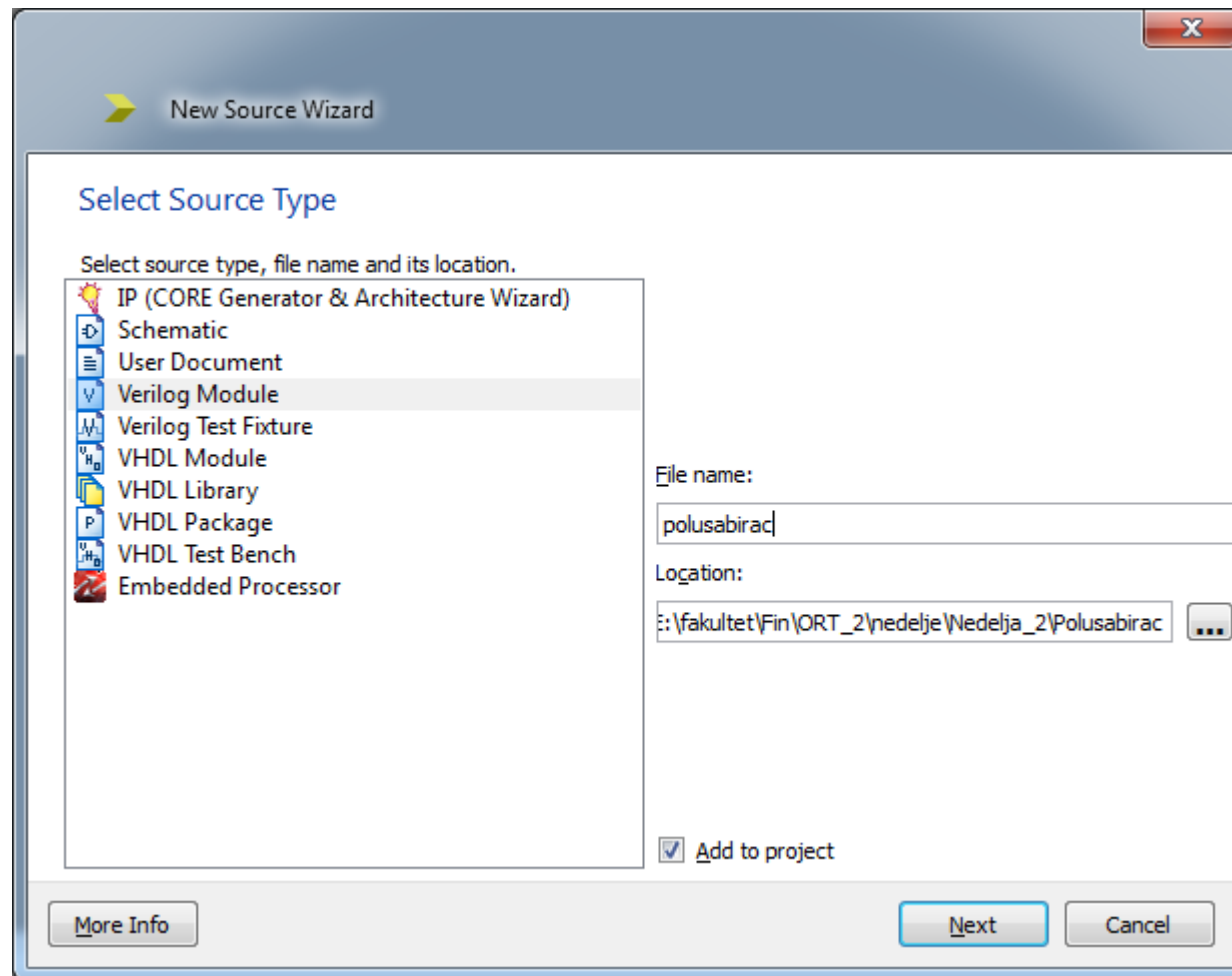
Polusabirac



Polusabirac



Polusabirac



Polusabirac

New Source Wizard

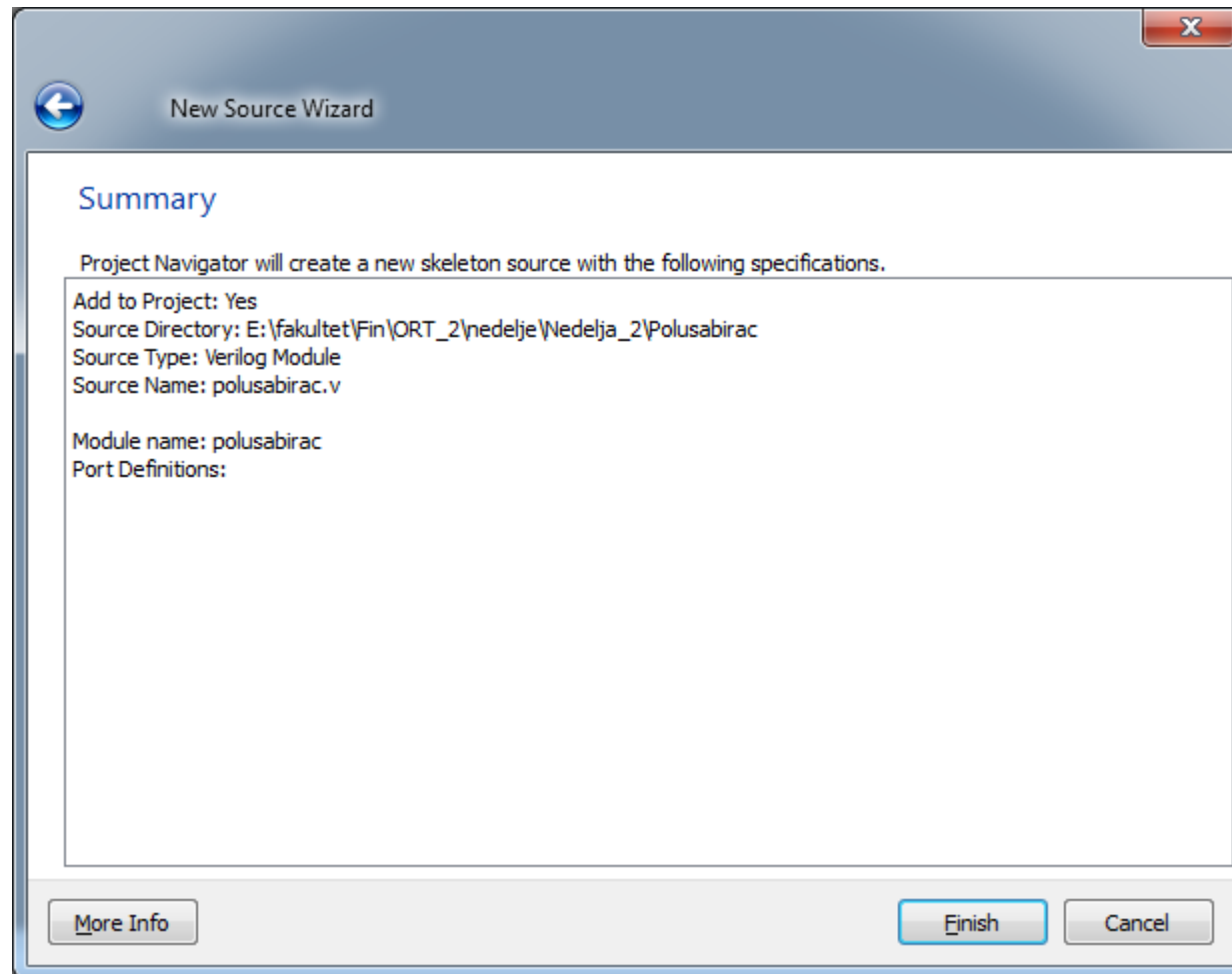
Define Module

Specify ports for module.

Module name

Port Name	Direction	Bus	MSB	LSB
	input	<input type="checkbox"/>		
	input	<input type="checkbox"/>		
	input	<input type="checkbox"/>		
	input	<input type="checkbox"/>		
	input	<input type="checkbox"/>		
	input	<input type="checkbox"/>		
	input	<input type="checkbox"/>		
	input	<input type="checkbox"/>		
	input	<input type="checkbox"/>		
	input	<input type="checkbox"/>		
	input	<input type="checkbox"/>		
	input	<input type="checkbox"/>		

Polusabirac



Polusabirac

The screenshot displays the Xilinx ISE Project Navigator interface. The main editor window shows the Verilog code for a module named 'polusabirac'. The code includes a timescale, comments, and a module definition.

```
1 `timescale 1ns / 1ps
2 ///////////////////////////////////////////////////////////////////
3 // Company:
4 // Engineer:
5 //
6 // Create Date:    10:19:16 10/10/2016
7 // Design Name:
8 // Module Name:   polusabirac
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ///////////////////////////////////////////////////////////////////
21 module polusabirac(
22     );
23
24
25 endmodule
26
```

The Design window on the left shows the Hierarchy view with the following structure:

- Polusabirac
 - xc3s1200e-5fg320
 - polusabirac (polusabirac.v)

The Console window at the bottom shows the following output:

```
Started : "Launching ISE Text Editor to edit polusabirac.v".
INFO:HDLCompiler:1845 - Analyzing Verilog file "E:/fakultet/Fin/ORT_2/nedelje/Nedelja_2/Polusabirac/polusabirac.v" into library work
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.
```

Polusabirac

ISE Project Navigator (P.20131013) - E:\fakultet\Fin\ORT_2\nedelje\Nedelja_2\Polusabirac\Polusabirac.xise - [polusabirac.v*]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementation Simulation

Behavioral

Hierarchy

- Polusabirac
 - xc3s1200e-5fg320
 - polusabirac (polusabirac.v)

No Processes Running

No single design module is selected.

Design Utilities

```
1 `timescale 1ns / 1ps
2 ///////////////////////////////////////////////////////////////////
3 // Company:
4 // Engineer:
5 //
6 // Create Date:    10:19:16 10/10/2016
7 // Design Name:
8 // Module Name:    polusabirac
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ///////////////////////////////////////////////////////////////////
21 module polusabirac(x, y, s, c);
22     input x, y;
23     output s, c;
24     xor(s, x, y);
25     and(c, x, y);
26
27 endmodule
28
```

Start Design Files Libraries

polusabirac.v*

Console

Started : "Launching ISE Text Editor to edit polusabirac.v".

INFO:HDLCompiler:1845 - Analyzing Verilog file "E:/fakultet/Fin/ORT_2/nedelje/Nedelja_2/Polusabirac/polusabirac.v" into library work

INFO:ProjectMgmt - Parsing design hierarchy completed successfully.

Console Errors Warnings Find in Files Results

Ln 24 Col 1 Verilog

Polusabirac

The screenshot displays the ISE Project Navigator interface. The main window shows a Verilog code editor with the following code:

```
1 `timescale 1ns / 1ps
2 ///////////////////////////////////////////////////////////////////
3 // Company:
4 // Engineer:
5 //
6 // Create Date:    10:19:16 10/10/2016
7 // Design Name:
8 // Module Name:    polusabirac
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ///////////////////////////////////////////////////////////////////
21 module polusabirac(x, y, s, c);
22     input x, y;
23     output s, c;
24     xor(s, x, y);
25     and(c, x, y);
26
27 endmodule
28
```

The left sidebar shows the Design view with the Hierarchy tree expanded to show the module `polusabirac (polusabirac.v)`. Below the hierarchy, the Processes list shows `ISim Simulator` with sub-processes `Behavioral Check Syntax` and `Simulate Behavioral Model`. A red arrow points from the `ISim Simulator` process to the console window.

The Console window at the bottom displays the following output:

```
Total time: 1 secs
Process "Generate Post-Place & Route Static Timing" completed successfully
```

The status bar at the bottom right indicates the current position is `Ln 24 Col 1` in a `Verilog` file.

Polusabirac

The screenshot displays the ISE Project Navigator interface. The main window shows a Verilog code editor with the following code:

```
1 `timescale 1ns / 1ps
2 ///////////////////////////////////////////////////////////////////
3 // Company:
4 // Engineer:
5 //
6 // Create Date:    10:19:16 10/10/2016
7 // Design Name:
8 // Module Name:    polusabirac
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ///////////////////////////////////////////////////////////////////
21 module polusabirac(x, y, s, c);
22     input x, y;
23     output s, c;
24     xor(s, x, y);
25     and(c, x, y);
26
27 endmodule
28
```

The left sidebar shows the Design view with the Hierarchy tree expanded to show the file `polusabirac (polusabirac.v)`. Below the hierarchy, the Processes section shows `ISim Simulator` with sub-items `Behavioral Check Syntax` and `Simulate Behavioral Model`. A red arrow points from the `Simulate Behavioral Model` item to the code editor. The Console window at the bottom shows the message: `Process "Generate Post-Place & Route Static Timing" completed successfully`.

Dupli klik

Polusabirac

ISim (P.20131013) - [Default.wcfg*]

File Edit View Simulation Window Layout Help

Instances and Processes

Instance and Process Name	Design Unit	Block Type
polusabirac	polusabirac	Verilog Module
gbl	gbl	Verilog Module

Simulation Object

Name	Value
x	Z
y	Z
s	X
c	X

Object Name

x
y
s
c

999,991 ps 999,992 ps 999,993 ps 999,994 ps 999,995 ps 999,996 ps 999,997 ps

X1: 999,992 ps

Instances and Processes Memory Source Files

Default.wcfg*

Console

WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>

Console Compilation Log Breakpoints Find in Files Results Search Results

Collapses the selected elements into its parent bus

Sim Time: 1,000,000 ps

Polusabirac

The screenshot shows the ISim (P.20131013) - [Default.wcfg*] window. The top menu includes File, Edit, View, Simulation, Window, Layout, and Help. The toolbar contains various simulation and editing tools. The main workspace is divided into several panes:

- Instances and Processes:** A table listing the design units and their block types.
- Simulation Object:** A tree view showing the hierarchy of simulation objects.
- Name/Value Table:** A table showing the current values of signals x, y, s, and c.
- Timing Diagram:** A waveform viewer showing the digital signals over time. A yellow vertical line is positioned at 999,992 ps.

Instance and Process Name	Design Unit	Block Type
polusabirac	polusabirac	Verilog Module
gbl	gbl	Verilog Module

Name	Value
x	z
y	z
s	x
c	x

Timing Diagram Data:

Time (ps)	x	y	s	c
999,991	z	z	x	x
999,992	z	z	x	x
999,993	z	z	x	x
999,994	z	z	x	x
999,995	z	z	x	x
999,996	z	z	x	x
999,997	z	z	x	x

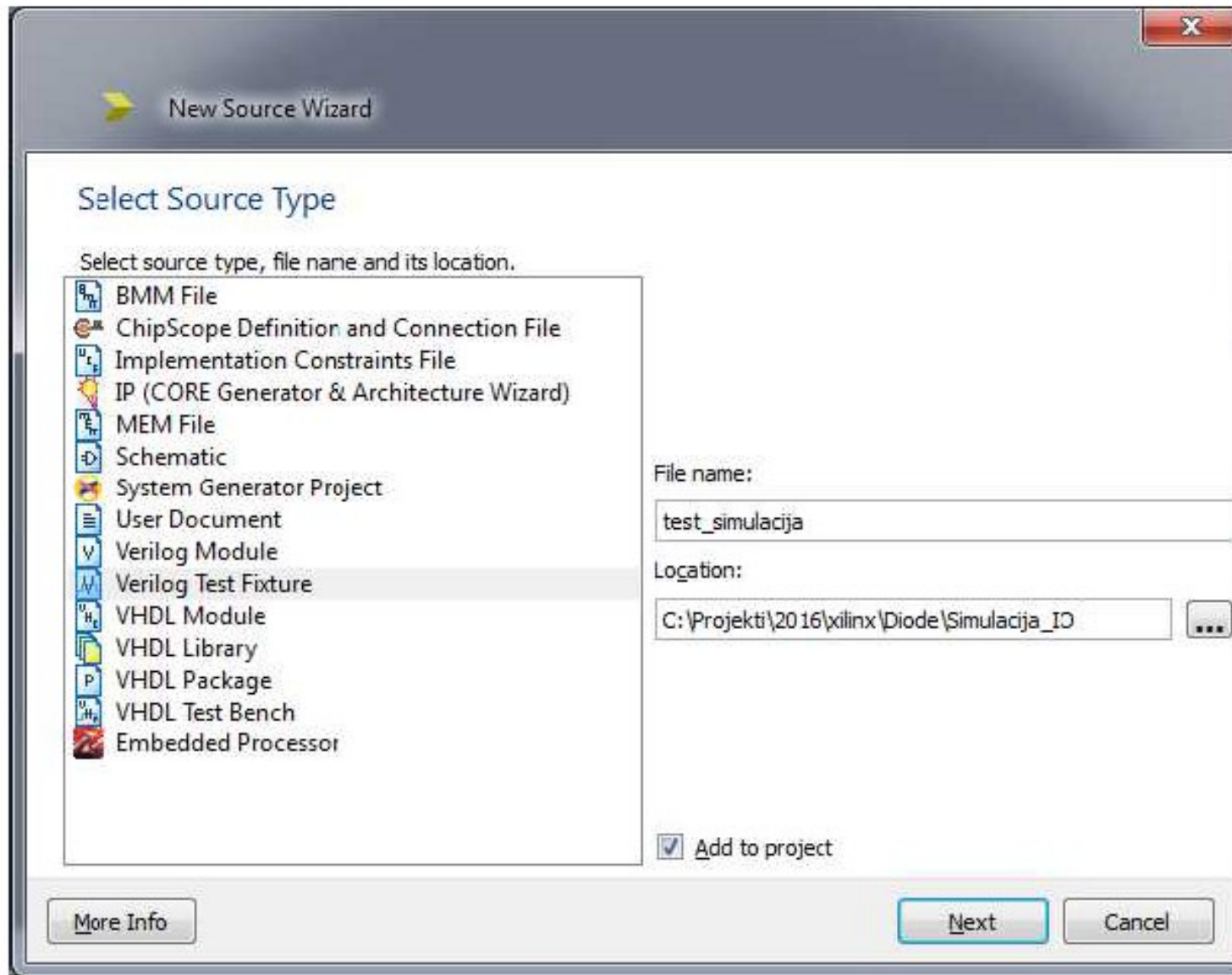
Console Output:

```
WARNING: A WEBPACK license was found.  
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.  
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.  
This is a Lite version of ISim.  
Time resolution is 1 ps  
Simulator is doing circuit initialization process.  
Finished circuit initialization process.  
ISim>
```

Bottom status bar: Collapses the selected elements into its parent bus. Sim Time: 1,000,000 ps

Definisanje parametara simulacije

Praktikum_ORT_1



Design View: Implementation Simulation Behavioral

Hierarchy

- Polusabirac
 - xc3s1200e-5fg320
 - polusabirac_simulator (polusabirac) (selected)
 - uut - polusabirac (polusabirac)

No Processes Running

Processes: polusabirac_simulator

- ISim Simulator
 - Behavioral Check Syntax
 - Simulate Behavioral Model

```
16 //
17 // Dependencies:
18 //
19 // Revision:
20 // Revision 0.01 - File Created
21 // Additional Comments:
22 //
23 ///////////////////////////////////////////////////////////////////
24
25 module polusabirac_simulator;
26
27     // Inputs
28     reg x;
29     reg y;
30
31     // Outputs
32     wire s;
33     wire c;
34
35     // Instantiate the Unit Under Test (UUT)
36     polusabirac uut (
37         .x(x),
38         .y(y),
39         .s(s),
40         .c(c)
41     );
42
43     initial begin
```

Console

ISim simulation engine GUI launched successfully

Process "Simulate Behavioral Model" completed successfully

ISE Project Navigator (P.20131013) - E:\fakultet\Fin\ORT_2\Nedelje\Nedelja_2\Polusabirac\Polusabirac.xise - [polusabirac_simulator.v]

File Edit View Project Source Process Tools Window Layout Help

Design View: Implementation Simulation Behavioral Hierarchy Polusabirac xc3s1200e-5fg320 polusabirac_simulator (polusabirac) uut - polusabirac (polusabirac)

```
16 //
17 // Dependencies:
18 //
19 // Revision:
20 // Revision 0.01 - File Created
21 // Additional Comments:
22 //
23 ///////////////////////////////////////////////////////////////////
24
25 module polusabirac_simulator;
26
27     // Inputs
28     reg x;
29     reg y;
```

ISE Project Navigator (P.20131013) - E:\fakultet\Fin\ORT_2\Nedelje\Nedelja_2\Polusabirac\Polusabirac.xise - [polusabirac_simulator.v]

File Edit View Project Source Process Tools Window Layout Help

Design View: Implementation Simulation Behavioral Hierarchy Polusabirac xc3s1200e-5fg320 polusabirac_simulator (polusabirac) uut - polusabirac (polusabirac)

No Processes Running

Processes: polusabirac_simulator

- ISim Simulator
- Behavioral Check Syntax
- Simulate Behavioral Model

```
40     .c(c)
41 );
42
43 initial begin
44     // Initialize Inputs
45     x = 0;
46     y = 0;
47     // Wait 100 ns for global reset to finish
48     #100;
49
50     x = 0;
51     y = 1;
52     #100;
53
54     x = 1;
55     y = 0;
56     #100;
57
58     x = 1;
59     y = 1;
60     // Wait 100 ns for global reset to finish
61     #100;
62
63 end
64
65 endmodule
66
67
```

Start Design Files Libraries

Design Summary (out of date) polusabirac_simulator.v

Console

```
ISim simulation engine GUI launched successfully
Process "Simulate Behavioral Model" completed successfully
```

Console Errors Warnings Find in Files Results

Definisanje parametara simulacije

The screenshot displays the ISim simulation environment. The main window shows a waveform plot with a time axis from 0 ns to 800 ns. The waveform contains four signals: 's' (a step function from 0 to 1 at 200 ns), 'c' (a step function from 0 to 1 at 400 ns), 'x' (a step function from 0 to 1 at 600 ns), and 'y' (a step function from 0 to 1 at 800 ns). A tooltip indicates the current time is 999.994 ns. The console window at the bottom displays the following text:

```
WARNING: A WEBPACK license was found.  
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.  
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.  
This is a Lite version of ISim.  
Time resolution is 1 ps  
Simulator is doing circuit initialization process.  
Finished circuit initialization process.  
ISim>
```

The console window also shows tabs for Console, Compilation Log, Breakpoints, Find in Files Results, and Search Results. The status bar at the bottom right indicates "Sim Time: 1,000,000 ps".