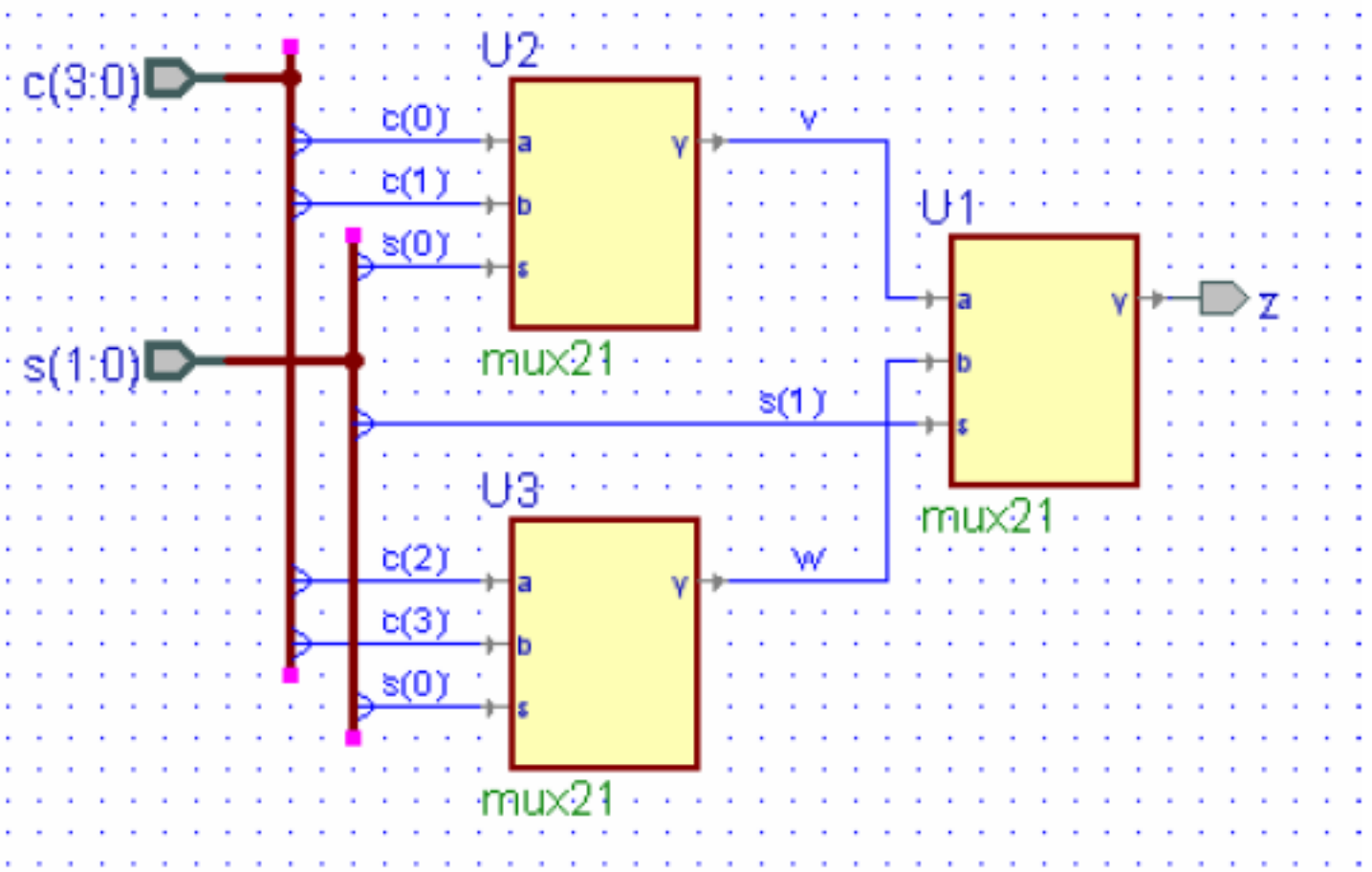
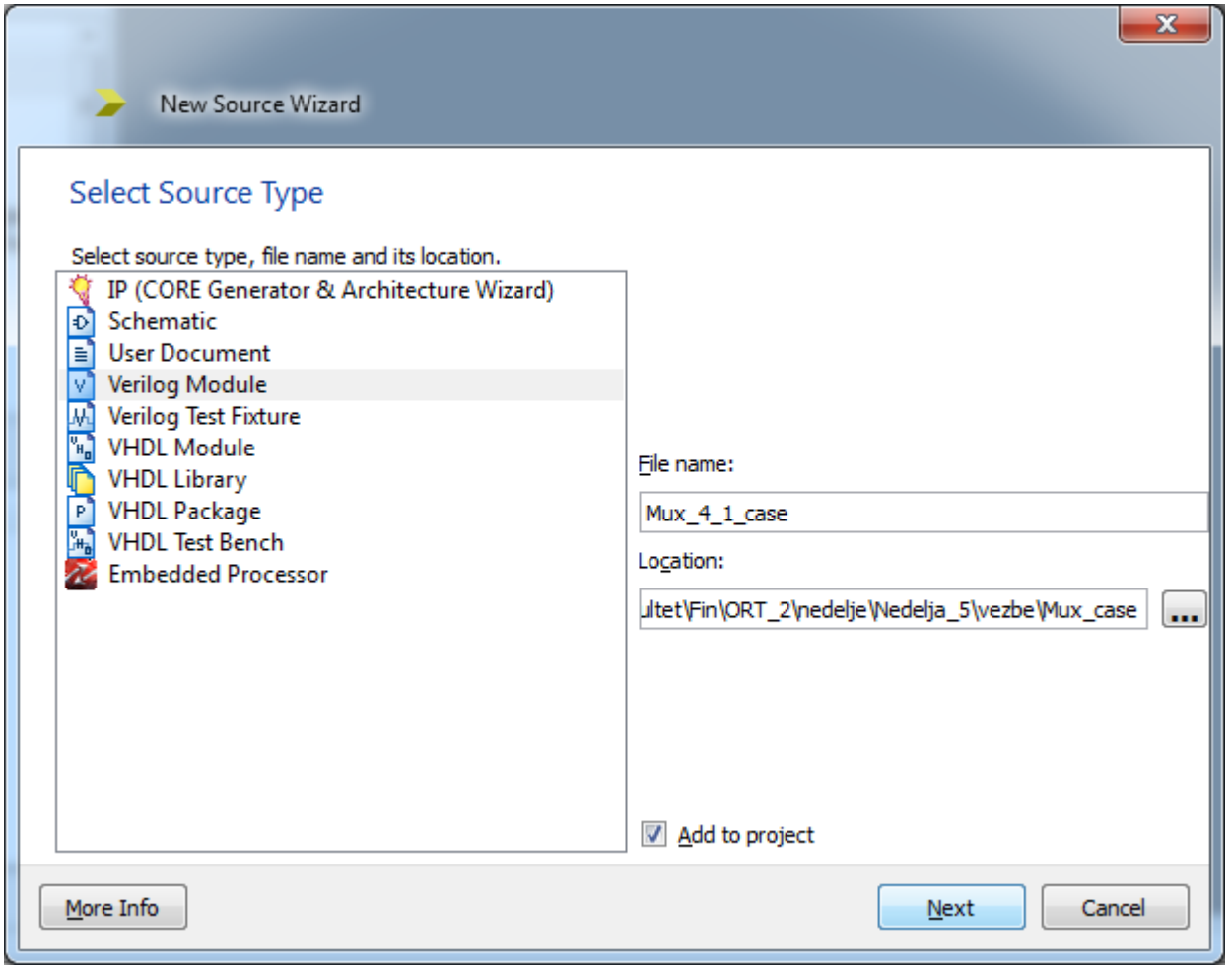
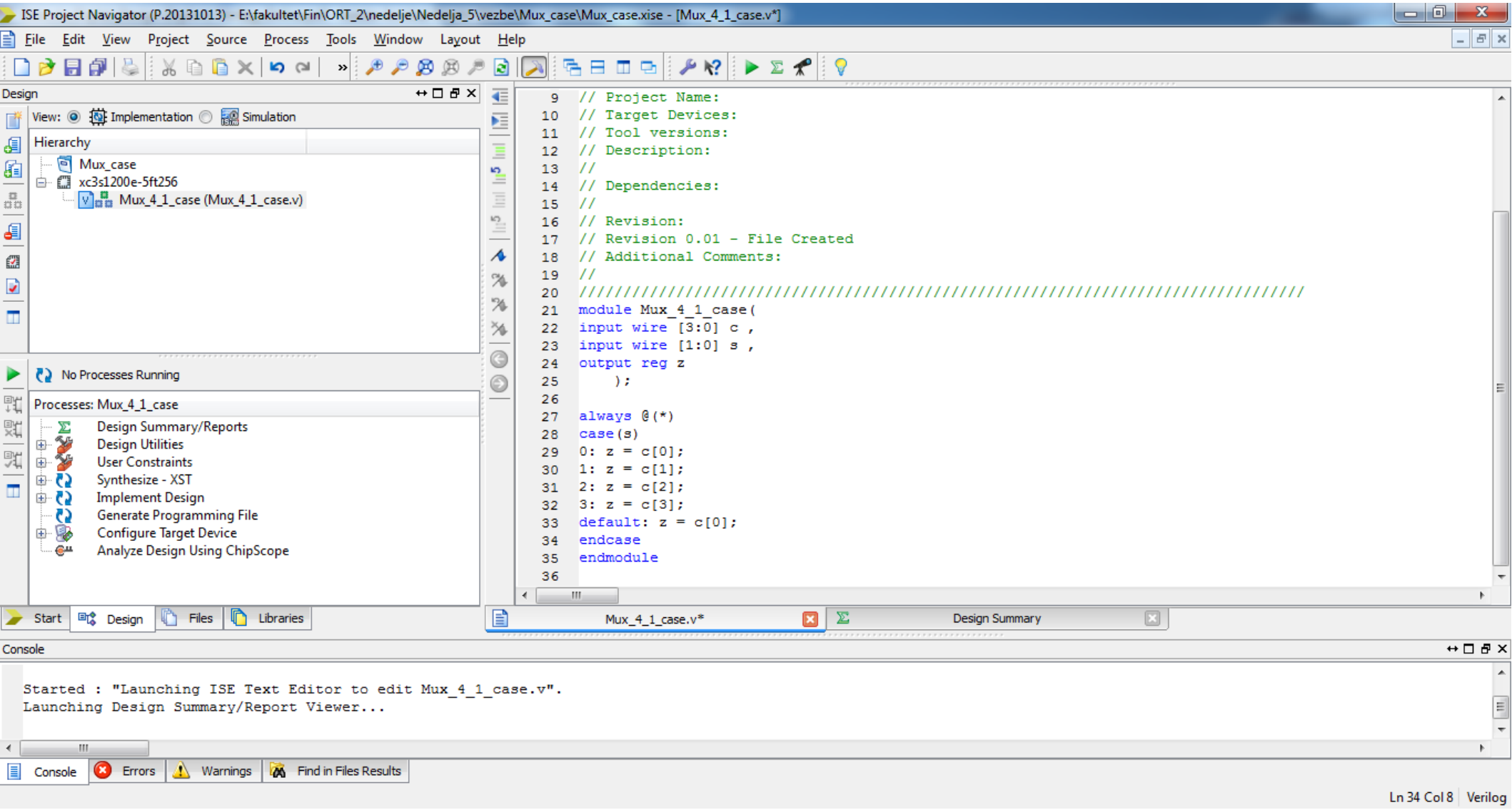
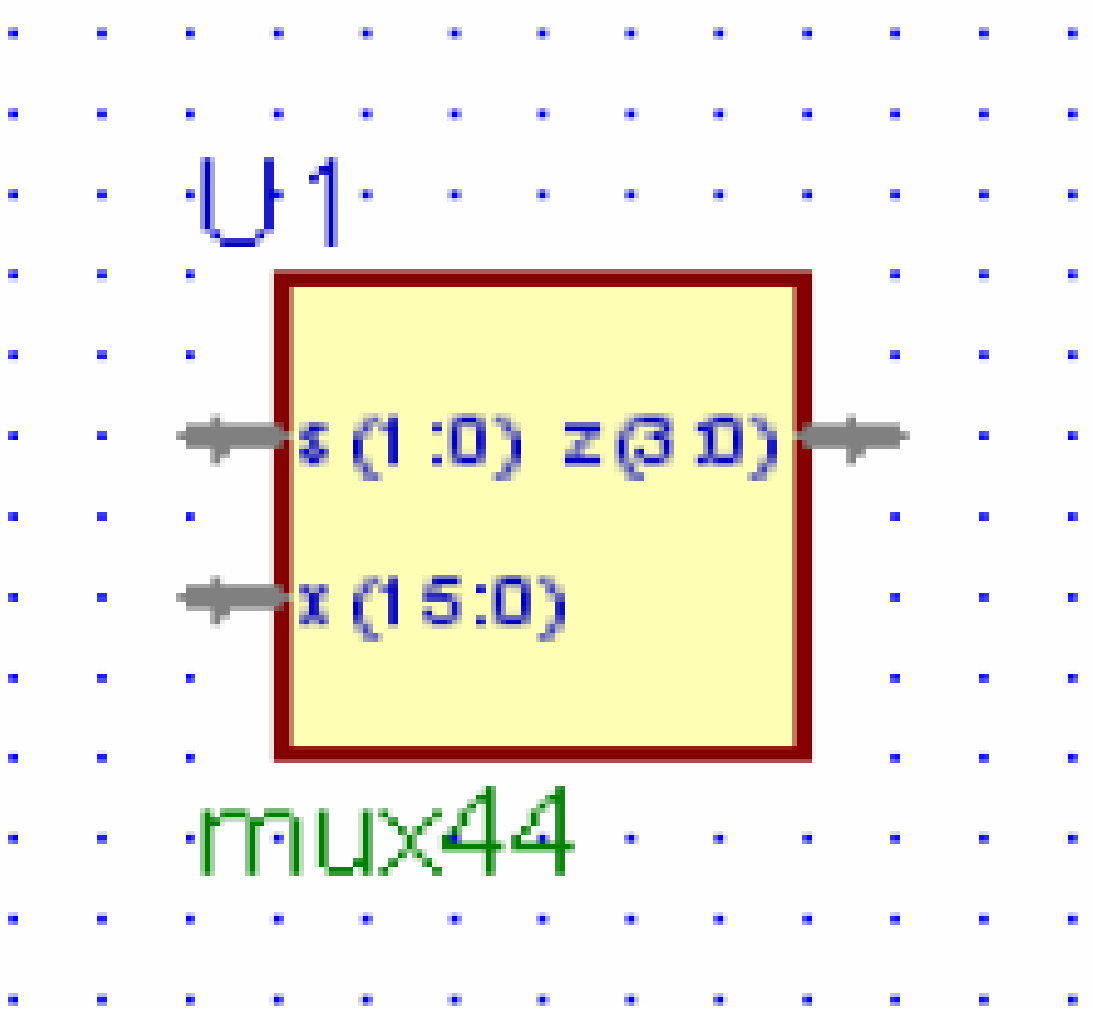
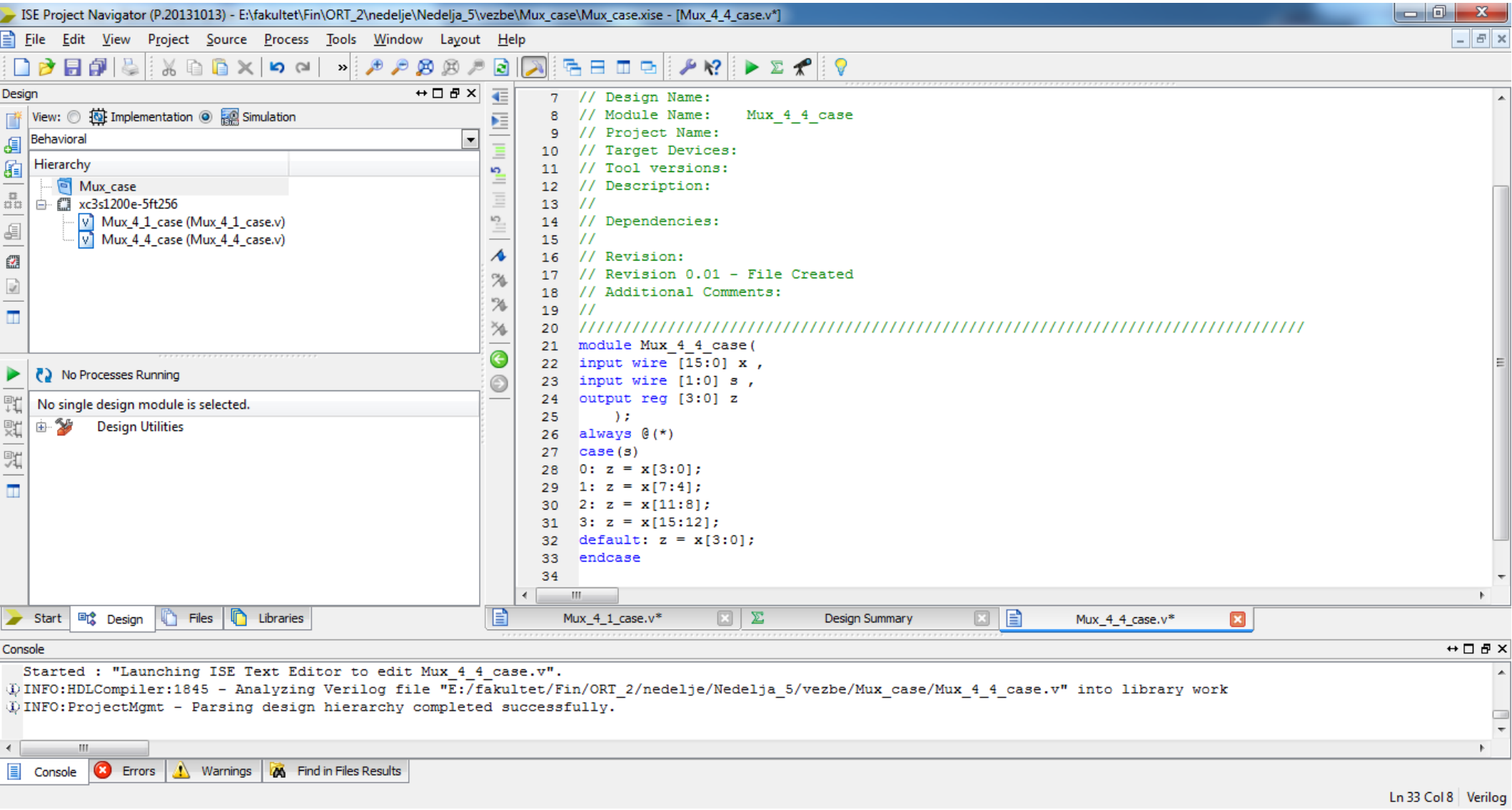

c(3:0)
s(1:0)
U2
c(0)
c(1)
s(0)
a
b
s
y
v
mux21
U1
a
b
s
y
z
s(1)
mux21
U3
c(2)
c(3)
s(0)
a
b
s
y
w
mux21

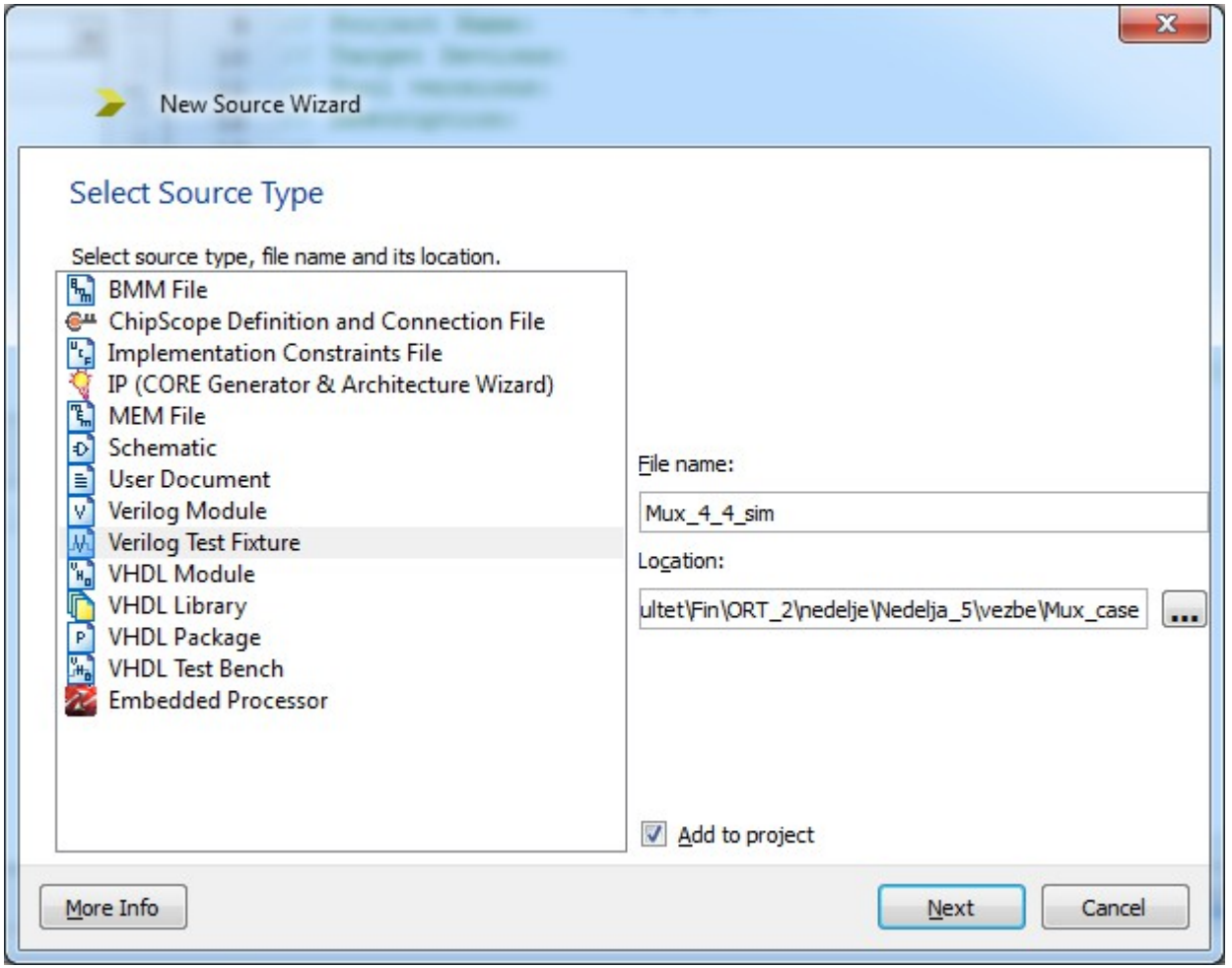

New Source Wizard
Select Source Type
Select source type, file name and its location.
IP (CORE Generator & Architecture Wizard)
Schematic
User Document
Verilog Module
Verilog Test Fixture
VHDL Module
VHDL Library
VHDL Package
VHDL Test Bench
Embedded Processor
File name:
Mux_4_1_case
Location:
ultet\Fin\ORT_2\nedelje\Nedelja_5\vezbe\Mux_case
...
Add to project
More Info
Next
Cancel

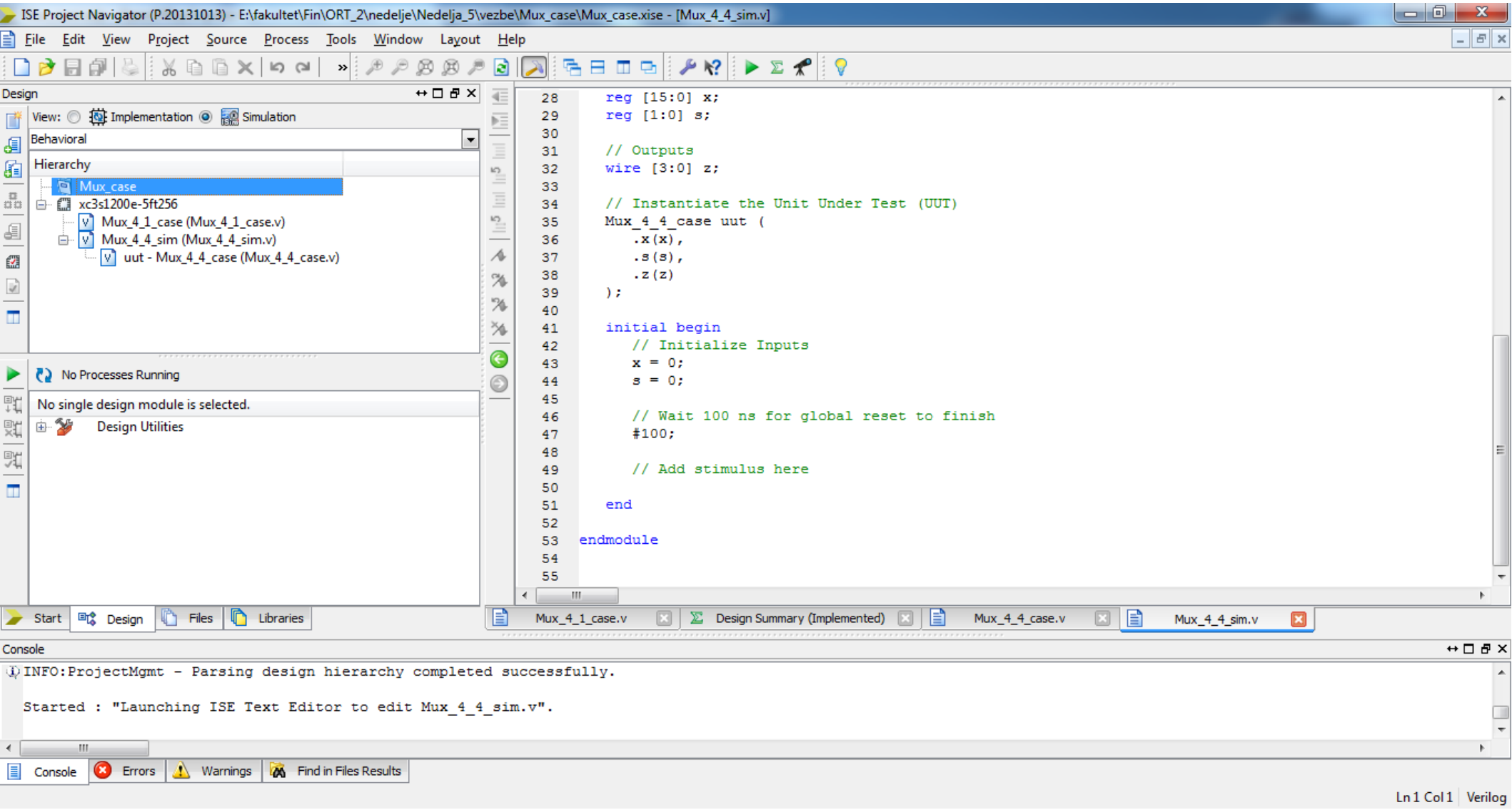

ISE Project Navigator (P.20131013) - E:\fakultet\Fin\ORT_2\nedelje\Nedelja_5\vezbe\Mux_case\Mux_case.xise - [Mux_4_1_case.v*]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
Mux_case
xc3s1200e-5ft256
Mux_4_1_case (Mux_4_1_case.v)
No Processes Running
Processes: Mux_4_1_case
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
Start Design Files Libraries
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////////////////////////////////////
21 module Mux_4_1_case(
22 input wire [3:0] c ,
23 input wire [1:0] s ,
24 output reg z
25 );
26
27 always @(*)
28 case(s)
29 0: z = c[0];
30 1: z = c[1];
31 2: z = c[2];
32 3: z = c[3];
33 default: z = c[0];
34 endcase
35 endmodule
36
Mux_4_1_case.v*
Design Summary
Console
Started : "Launching ISE Text Editor to edit Mux_4_1_case.v".
Launching Design Summary/Report Viewer...
Console Errors Warnings Find in Files Results
Ln 34 Col 8 Verilog

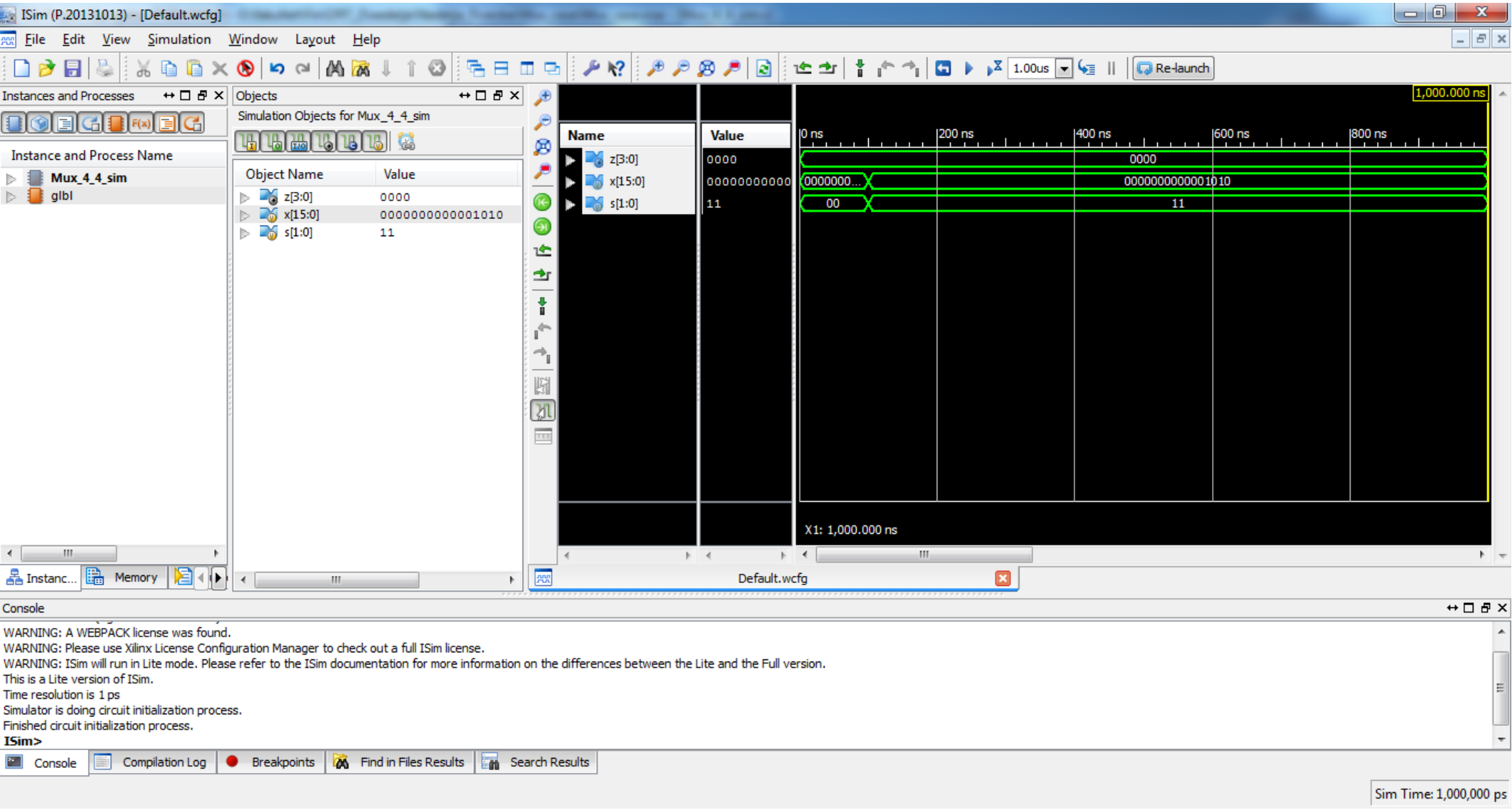
Za 4 4_1 mux moze da se kombinuje 4x 4_1 mux, probati
Koristecnjem case uslova, moze se kreirati 4x4 mux


U1
s (1 :0)
z (3 :0)
x (1 5:0)
mux44


ISE Project Navigator (P.20131013) - E:\fakultet\Fin\ORT_2\nedelje\Nedelja_5\vezbe\Mux_case\Mux_case.xise - [Mux_4_4_case.v*]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
Mux_case
xc3s1200e-5ft256
Mux_4_1_case (Mux_4_1_case.v)
Mux_4_4_case (Mux_4_4_case.v)
No Processes Running
No single design module is selected.
Design Utilities
7 // Design Name:
8 // Module Name: Mux_4_4_case
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////////////////////////////////////
21 module Mux_4_4_case(
22 input wire [15:0] x ,
23 input wire [1:0] s ,
24 output reg [3:0] z
25 );
26 always @(*)
27 case(s)
28 0: z = x[3:0];
29 1: z = x[7:4];
30 2: z = x[11:8];
31 3: z = x[15:12];
32 default: z = x[3:0];
33 endcase
34
Start Design Files Libraries
Mux_4_1_case.v*
Design Summary
Mux_4_4_case.v*
Console
Started : "Launching ISE Text Editor to edit Mux_4_4_case.v".
INFO:HDLCompiler:1845 - Analyzing Verilog file "E:/fakultet/Fin/ORT_2/nedelje/Nedelja_5/vezbe/Mux_case/Mux_4_4_case.v" into library work
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.
Console Errors Warnings Find in Files Results
Ln 33 Col 8 Verilog


New Source Wizard
Select Source Type
Select source type, file name and its location.
BMM File
ChipScope Definition and Connection File
Implementation Constraints File
IP (CORE Generator & Architecture Wizard)
MEM File
Schematic
User Document
Verilog Module
Verilog Test Fixture
VHDL Module
VHDL Library
VHDL Package
VHDL Test Bench
Embedded Processor
File name:
Mux_4_4_sim
Location:
ultet\Fin\ORT_2\nedelje\Nedelja_5\vezbe\Mux_case
...
Add to project
More Info
Next
Cancel


ISE Project Navigator (P.20131013) - E:\fakultet\Fin\ORT_2\nedelje\Nedelja_5\vezbe\Mux_case\Mux_case.xise - [Mux_4_4_sim.v]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
Mux_case
xc3s1200e-5ft256
Mux_4_1_case (Mux_4_1_case.v)
Mux_4_4_sim (Mux_4_4_sim.v)
uut - Mux_4_4_case (Mux_4_4_case.v)
No Processes Running
No single design module is selected.
Design Utilities
28 reg [15:0] x;
29 reg [1:0] s;
30
31 // Outputs
32 wire [3:0] z;
33
34 // Instantiate the Unit Under Test (UUT)
35 Mux_4_4_case uut (
36 .x(x),
37 .s(s),
38 .z(z)
39 );
40
41 initial begin
42 // Initialize Inputs
43 x = 0;
44 s = 0;
45
46 // Wait 100 ns for global reset to finish
47 #100;
48
49 // Add stimulus here
50
51 end
52
53 endmodule
54
55
Start Design Files Libraries
Mux_4_1_case.v
Design Summary (Implemented)
Mux_4_4_case.v
Mux_4_4_sim.v
Console
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.
Started : "Launching ISE Text Editor to edit Mux_4_4_sim.v".
Console Errors Warnings Find in Files Results
Ln 1 Col 1 Verilog


ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
1.00us
Instances and Processes
Instance and Process Name
Mux_4_4_sim
glbl
Objects
Simulation Objects for Mux_4_4_sim
Object Name
Value
z[3:0]
0000
x[15:0]
0000000000001010
s[1:0]
11
Name
Value
z[3:0]
0000
x[15:0]
0000000000001010
s[1:0]
11
1,000.000 ns
0 ns
200 ns
400 ns
600 ns
800 ns
0000
0000000...
00
11
X1: 1,000.000 ns
Instanc...
Memory
Default.wcfg
Console
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps