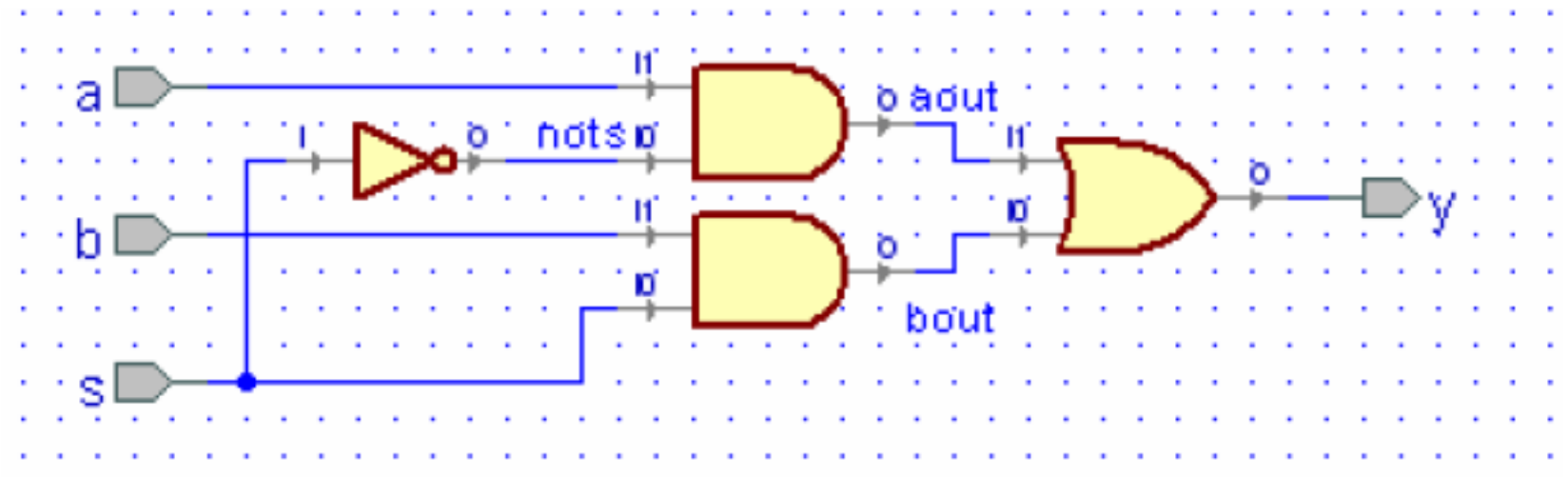
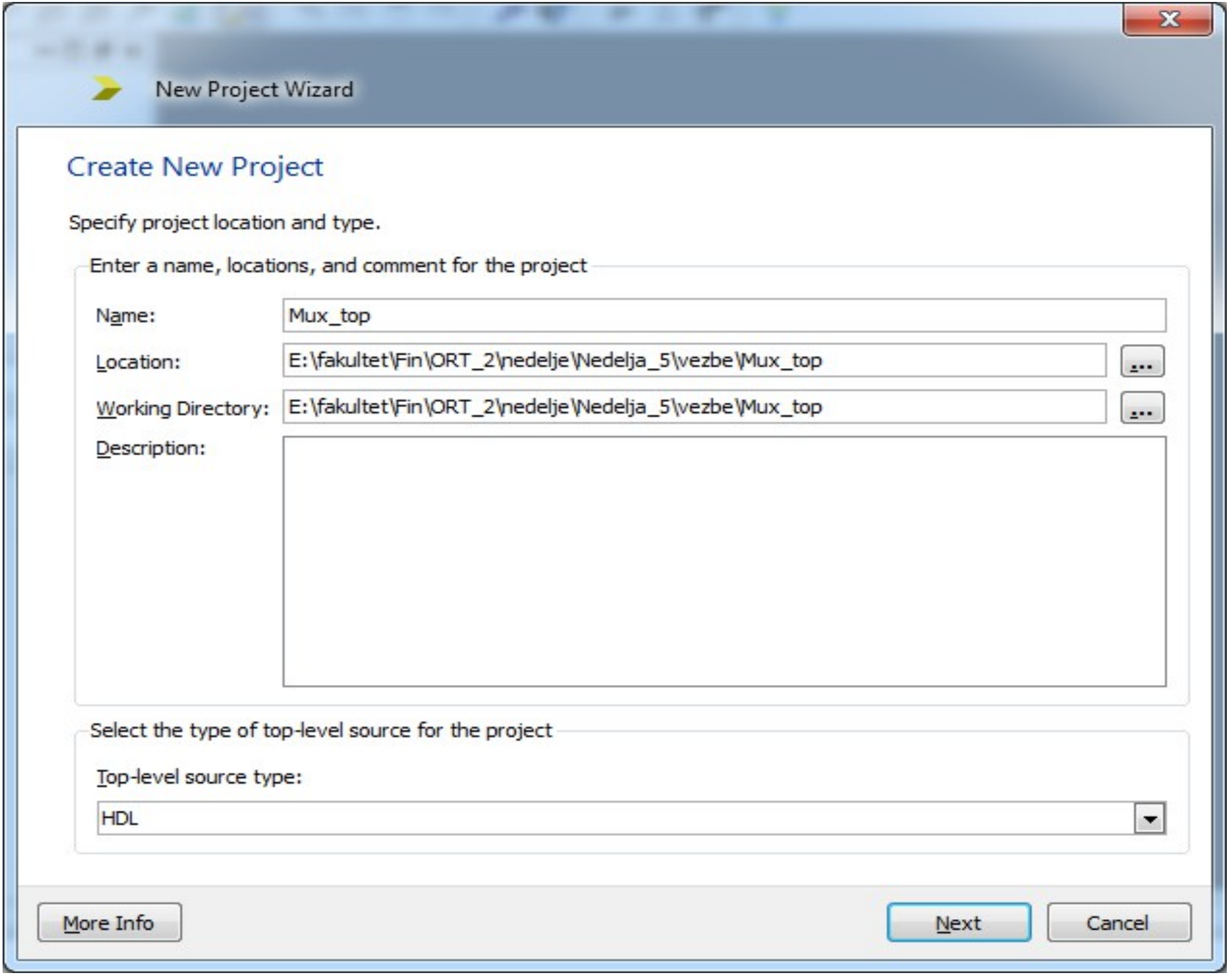
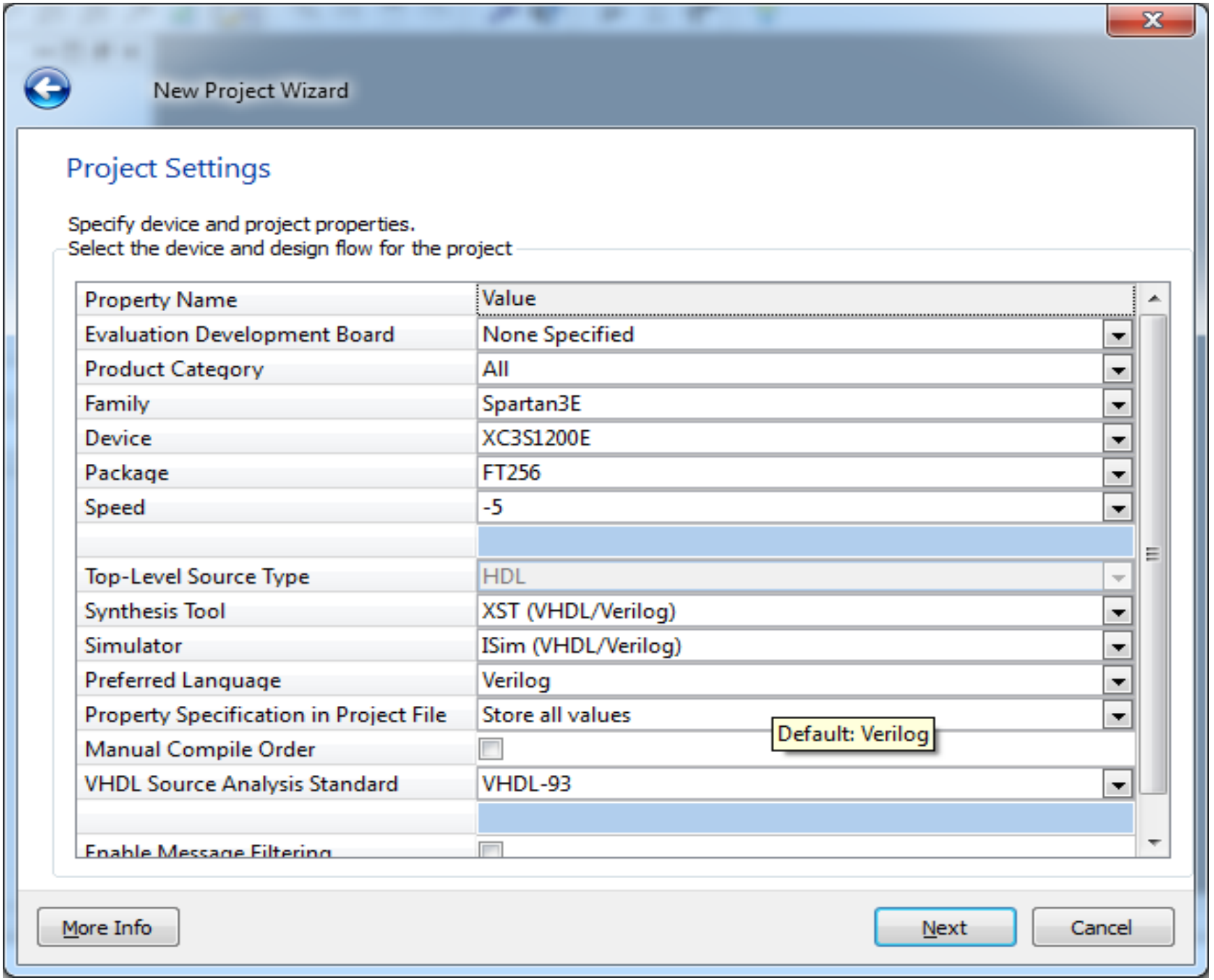
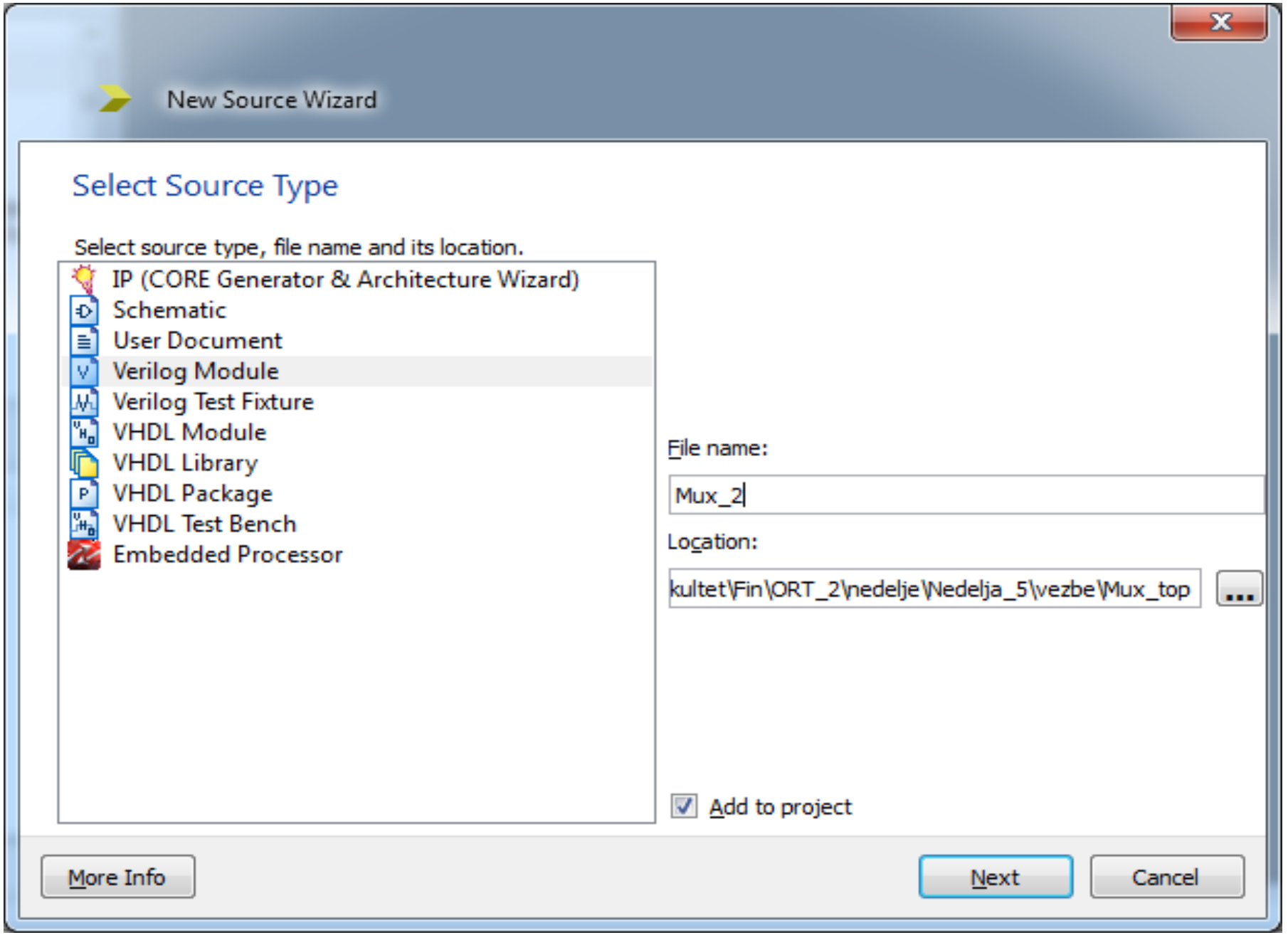
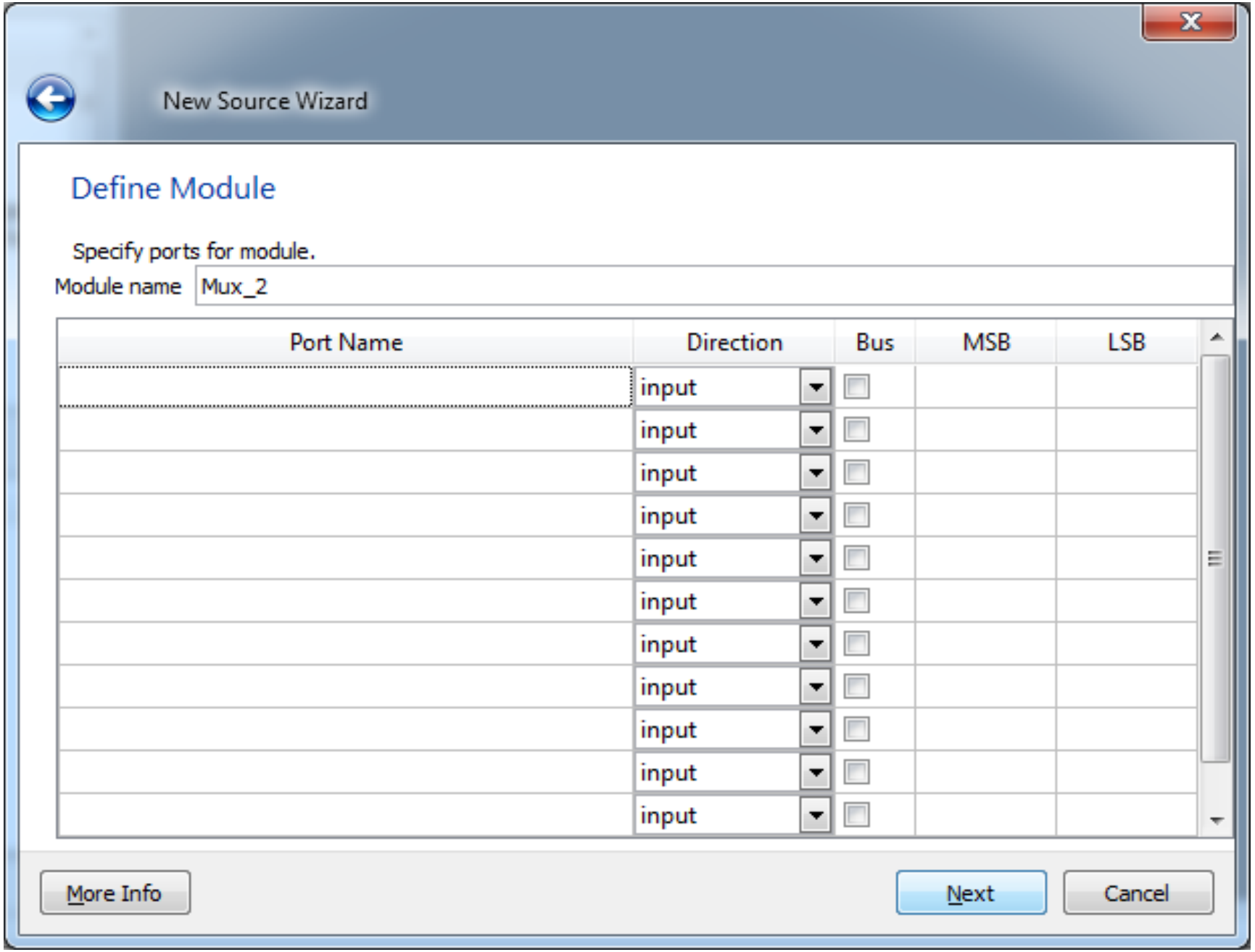

a
b
s
i
o
nots
i1
i0
o aout
i1
i0
o
bout
o
y

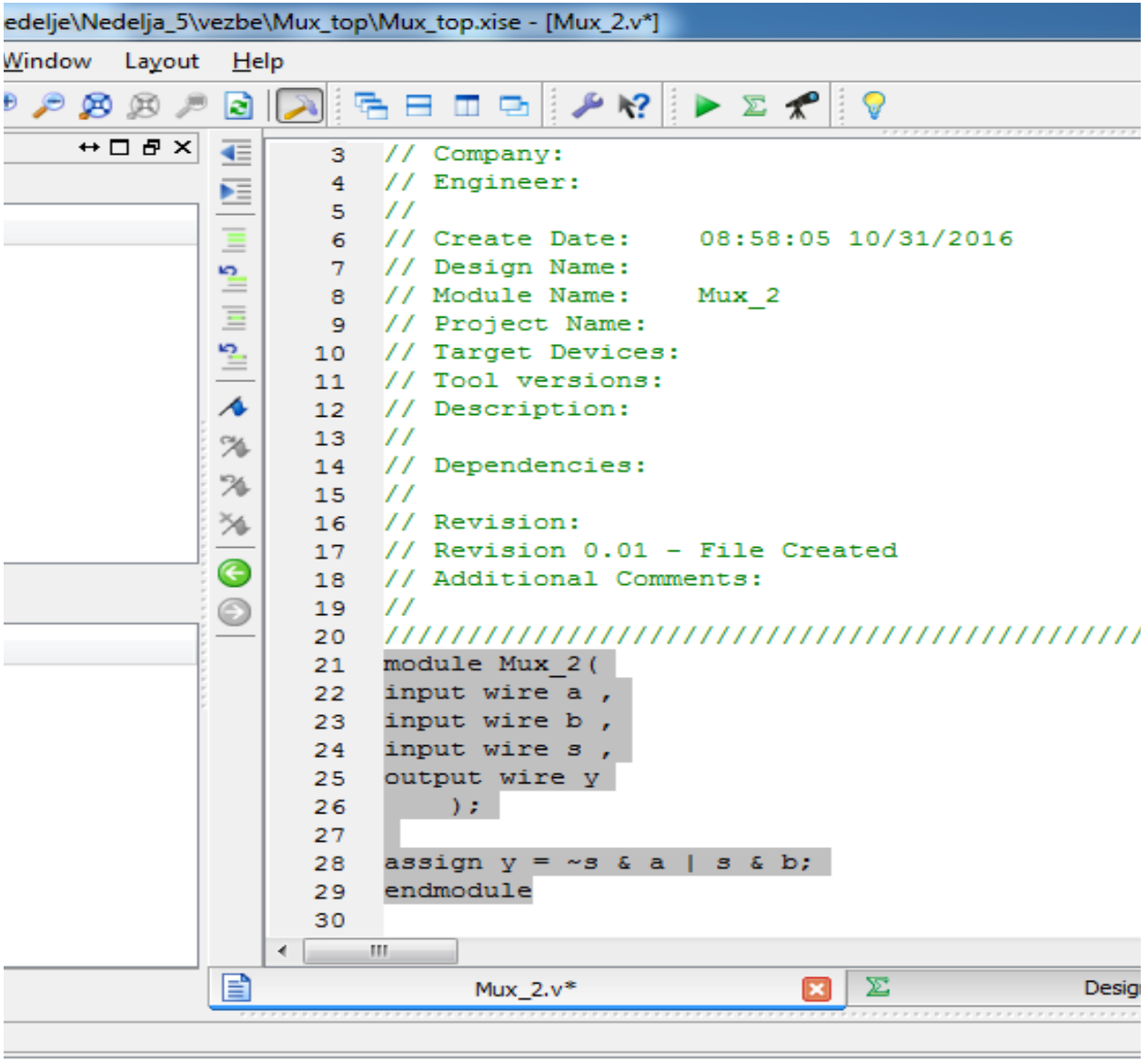

New Project Wizard
Create New Project
Specify project location and type.
Enter a name, locations, and comment for the project
Name:
Mux_top
Location:
E:\fakultet\Fin\ORT_2\nedelje\Nedelja_5\vezbe\Mux_top
Working Directory:
E:\fakultet\Fin\ORT_2\nedelje\Nedelja_5\vezbe\Mux_top
Description:
Select the type of top-level source for the project
Top-level source type:
HDL
More Info
Next
Cancel

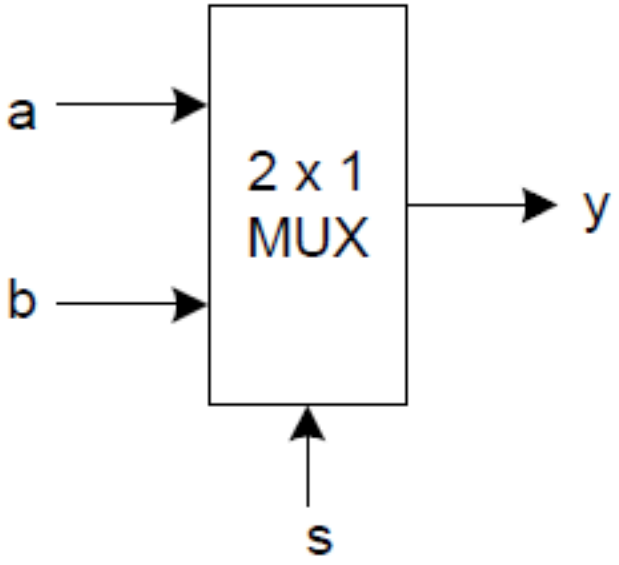

New Project Wizard
Project Settings
Specify device and project properties.
Select the device and design flow for the project
Property Name
Value
Evaluation Development Board
None Specified
Product Category
All
Family
Spartan3E
Device
XC3S1200E
Package
FT256
Speed
-5
Top-Level Source Type
HDL
Synthesis Tool
XST (VHDL/Verilog)
Simulator
ISim (VHDL/Verilog)
Preferred Language
Verilog
Property Specification in Project File
Store all values
Default: Verilog
Manual Compile Order
VHDL Source Analysis Standard
VHDL-93
Enable Message Filtering
More Info
Next
Cancel


New Source Wizard
Select Source Type
Select source type, file name and its location.
IP (CORE Generator & Architecture Wizard)
Schematic
User Document
Verilog Module
Verilog Test Fixture
VHDL Module
VHDL Library
VHDL Package
VHDL Test Bench
Embedded Processor
File name:
Mux_2
Location:
kultet\Fin\ORT_2\nedelje\Nedelja_5\vezbe\Mux_top
...
Add to project
More Info
Next
Cancel


New Source Wizard
Define Module
Specify ports for module.
Module name
Mux_2
Port Name
Direction
Bus
MSB
LSB
input
More Info
Next
Cancel

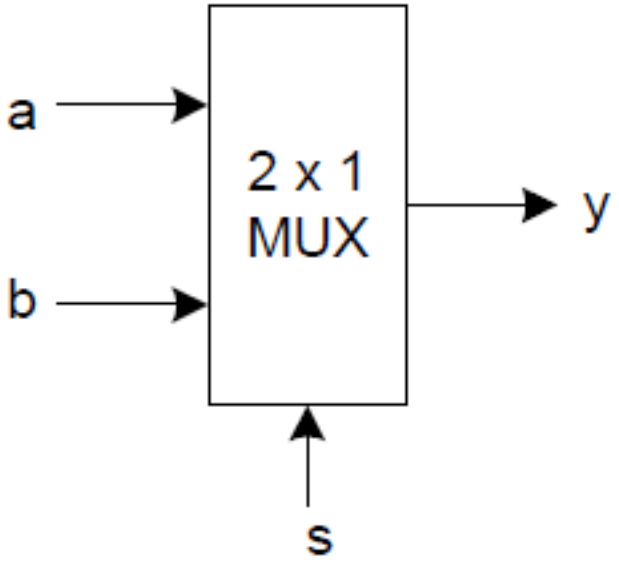
Samo Next


edelje\Nedelja_5\vezbe\Mux_top\Mux_top.xise - [Mux_2.v*]
Window Layout Help
3 // Company:
4 // Engineer:
5 //
6 // Create Date: 08:58:05 10/31/2016
7 // Design Name:
8 // Module Name: Mux_2
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21 module Mux_2(
22 input wire a ,
23 input wire b ,
24 input wire s ,
25 output wire y
26);
27
28 assign y = ~s & a | s & b;
29 endmodule
30
Mux_2.v*
Desig
edit Mux_2.v".
.
sults



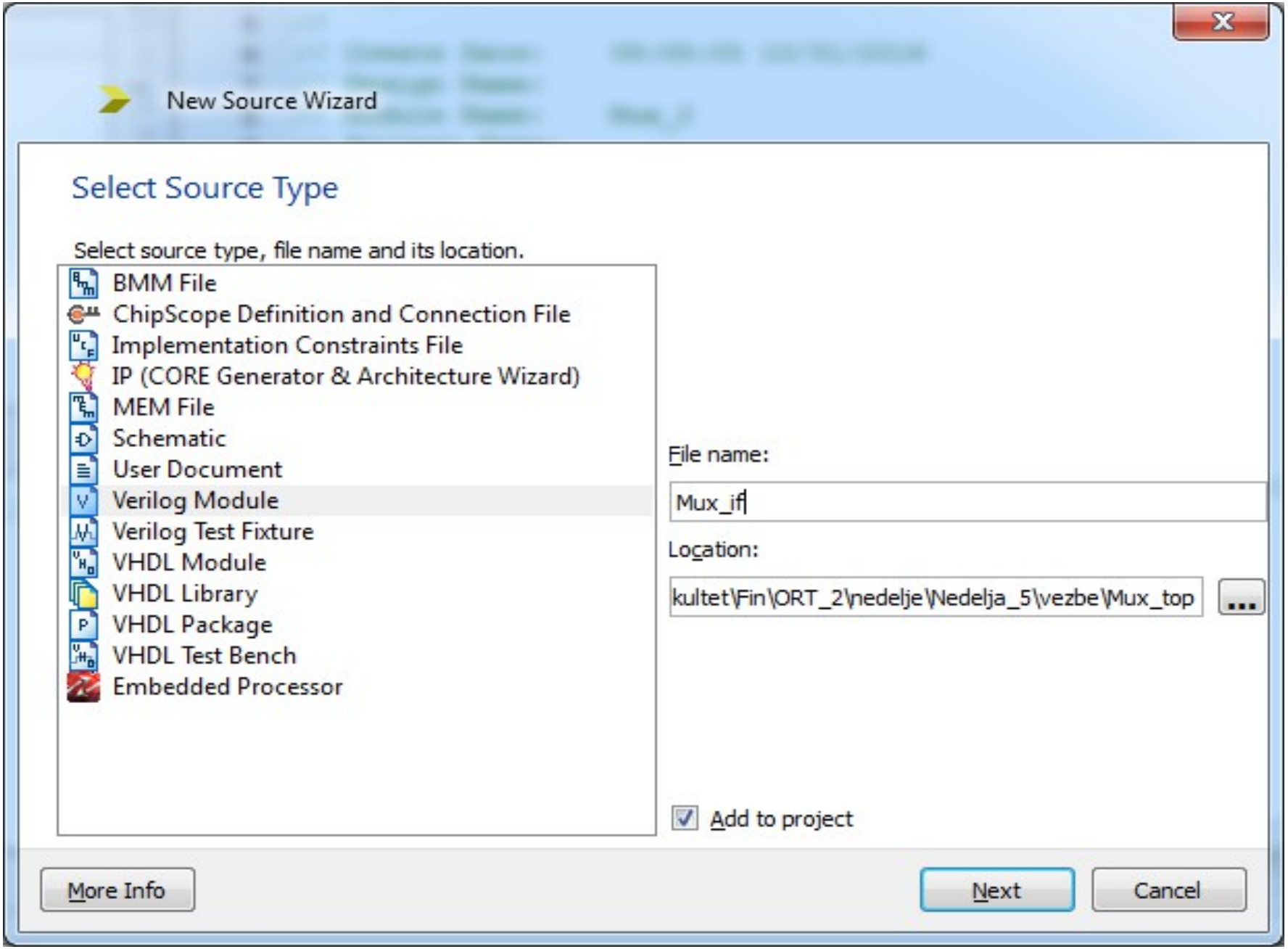
s	a	b	y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

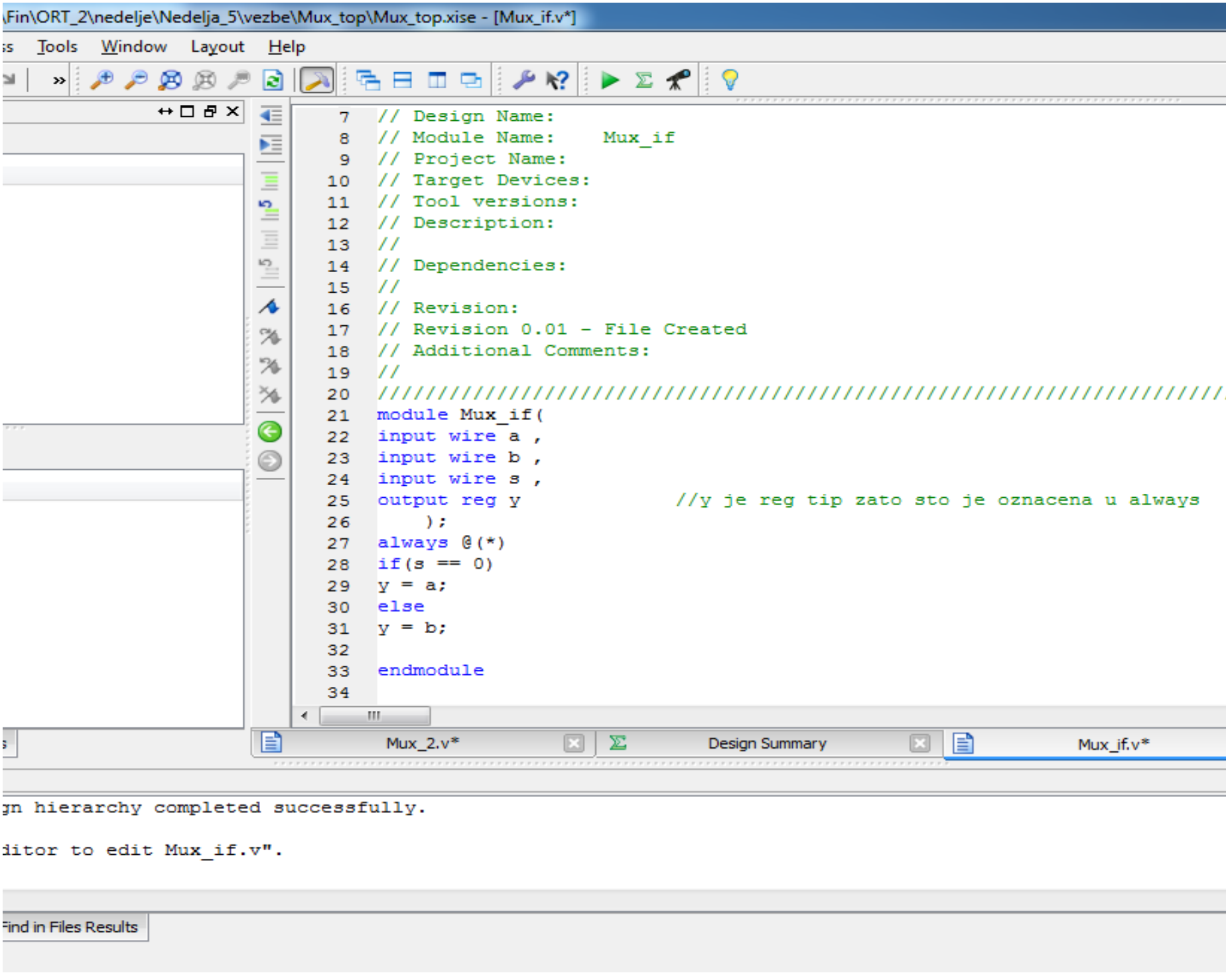
```
if(s == 0)
   y = a;
else
   y = b;
```

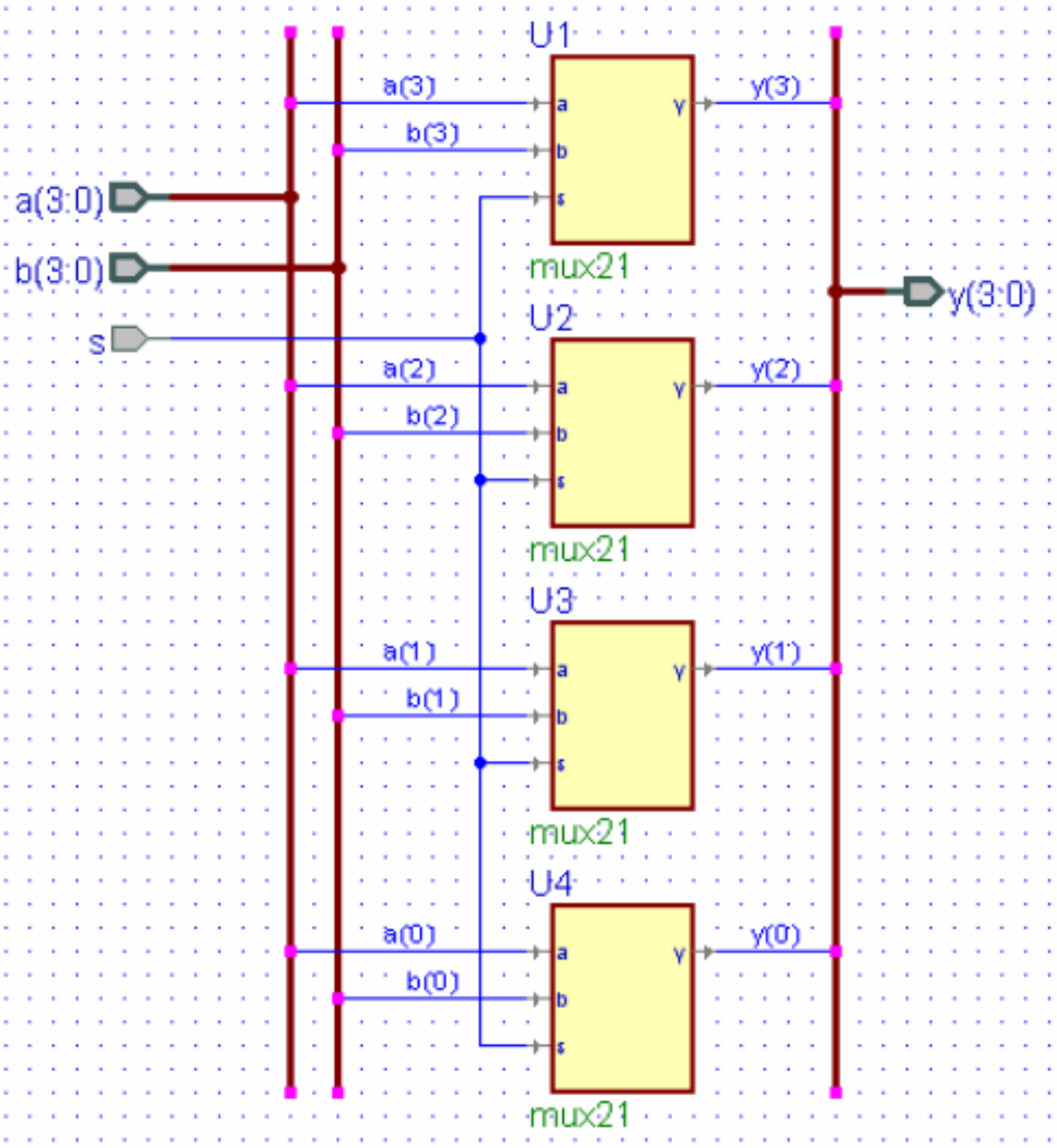


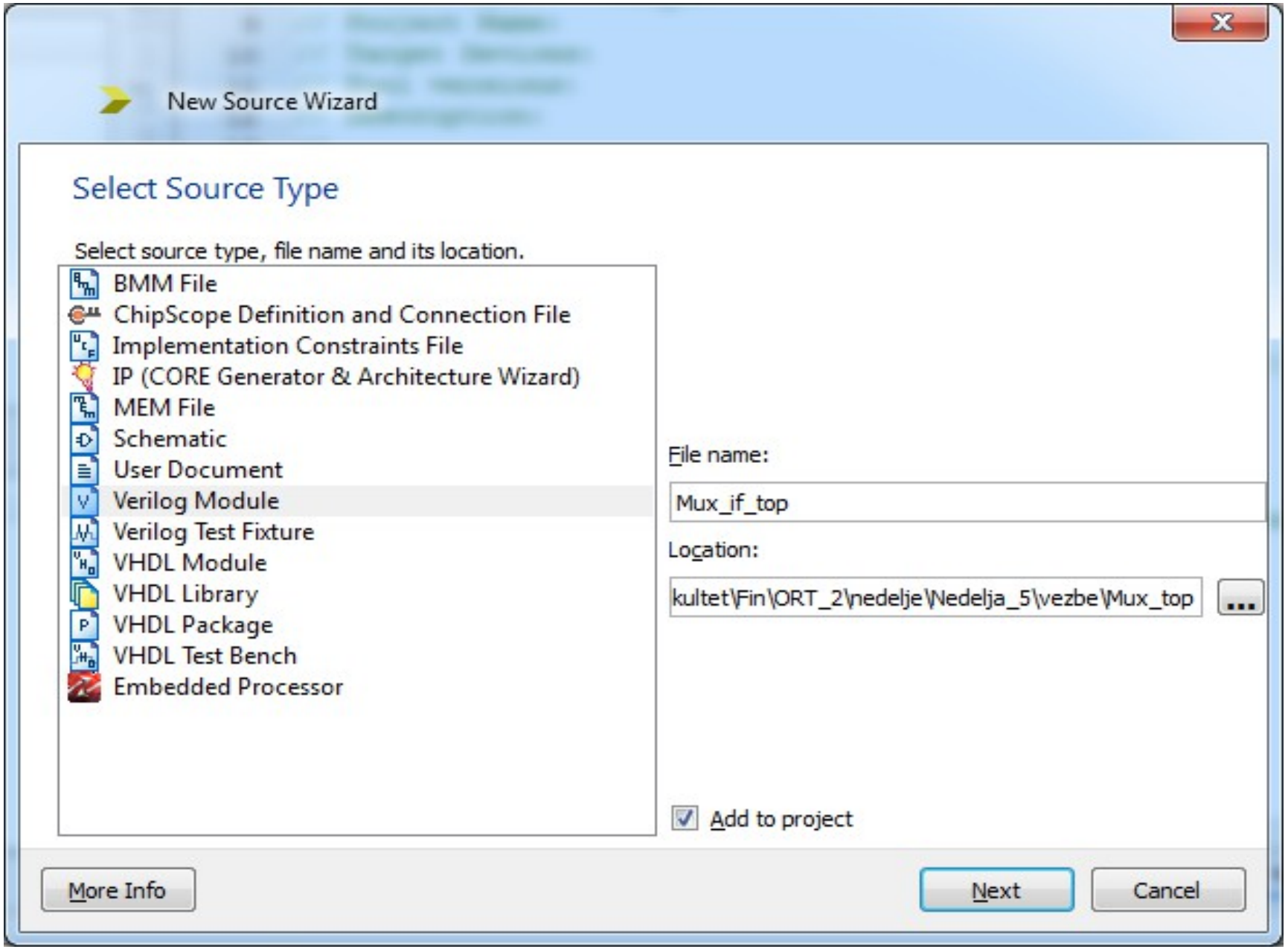
s	a	b	y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

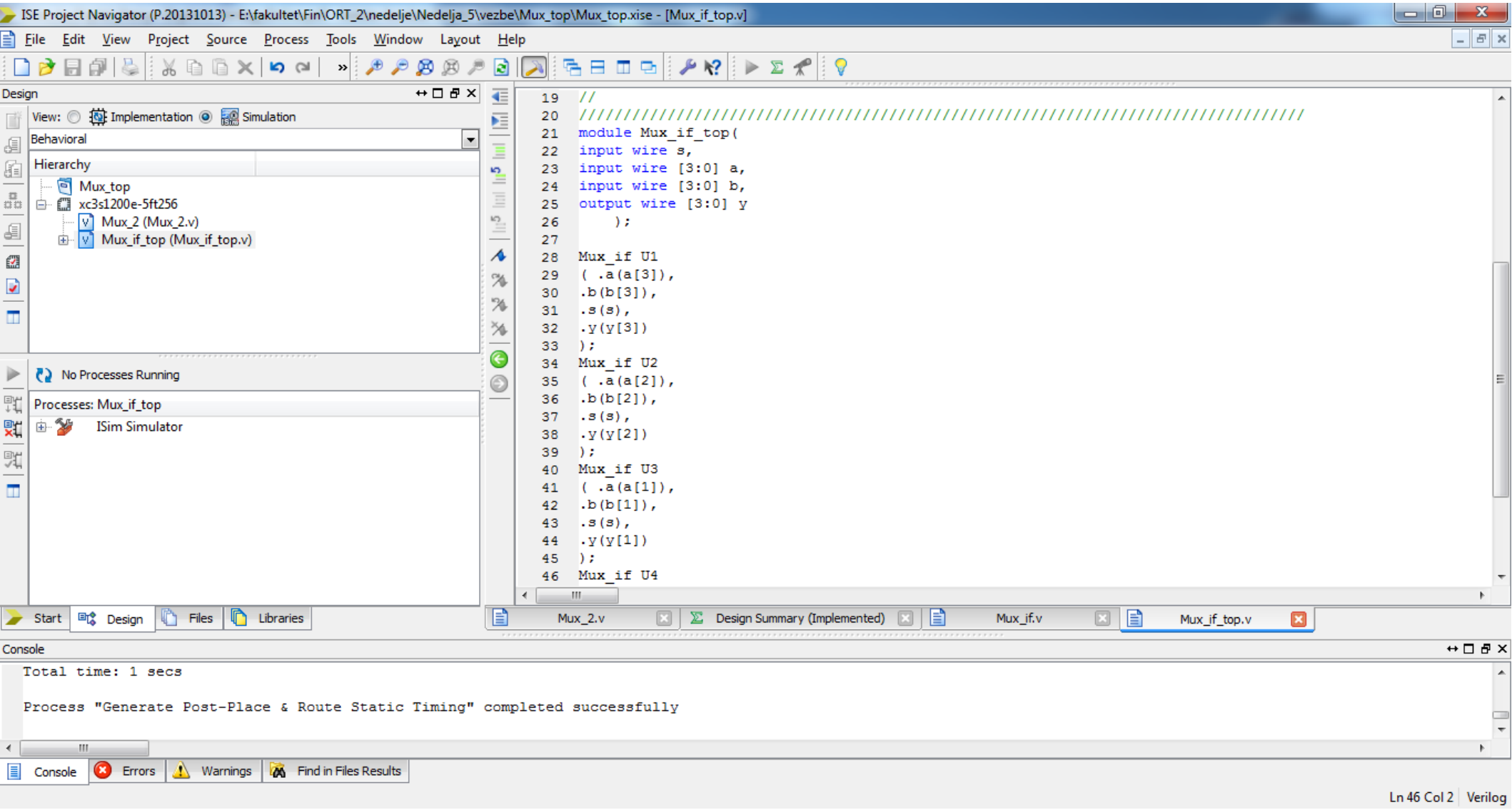
```
if(s == 0)
   y = a;
else
   y = b;
```


New Source Wizard
Select Source Type
Select source type, file name and its location.
BMM File
ChipScope Definition and Connection File
Implementation Constraints File
IP (CORE Generator & Architecture Wizard)
MEM File
Schematic
User Document
Verilog Module
Verilog Test Fixture
VHDL Module
VHDL Library
VHDL Package
VHDL Test Bench
Embedded Processor
File name:
Mux_if
Location:
kultet\Fin\ORT_2\nedelje\Nedelja_5\vezbe\Mux_top
...
Add to project
More Info
Next
Cancel


\Fin\ORT_2\nedelje\Nedelja_5\vezbe\Mux_top\Mux_top.xise - [Mux_if.v*]
Tools
Window
Layout
Help
// Design Name:
// Module Name: Mux_if
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
module Mux_if(
input wire a ,
input wire b ,
input wire s ,
output reg y //y je reg tip zato sto je oznacena u always
);
always @(*)
if(s == 0)
y = a;
else
y = b;
endmodule
Mux_2.v*
Design Summary
Mux_if.v*
gn hierarchy completed successfully.
ditor to edit Mux_if.v".
Find in Files Results


U1
a(3)
b(3)
a
b
s
y
y(3)
mux21
a(3:0)
b(3:0)
s
y(3:0)
U2
a(2)
b(2)
y(2)
mux21
U3
a(1)
b(1)
y(1)
mux21
U4
a(0)
b(0)
y(0)
mux21


New Source Wizard
Select Source Type
Select source type, file name and its location.
BMM File
ChipScope Definition and Connection File
Implementation Constraints File
IP (CORE Generator & Architecture Wizard)
MEM File
Schematic
User Document
Verilog Module
Verilog Test Fixture
VHDL Module
VHDL Library
VHDL Package
VHDL Test Bench
Embedded Processor
File name:
Mux_if_top
Location:
kultet\Fin\ORT_2\nedelje\Nedelja_5\vezbe\Mux_top
...
Add to project
More Info
Next
Cancel



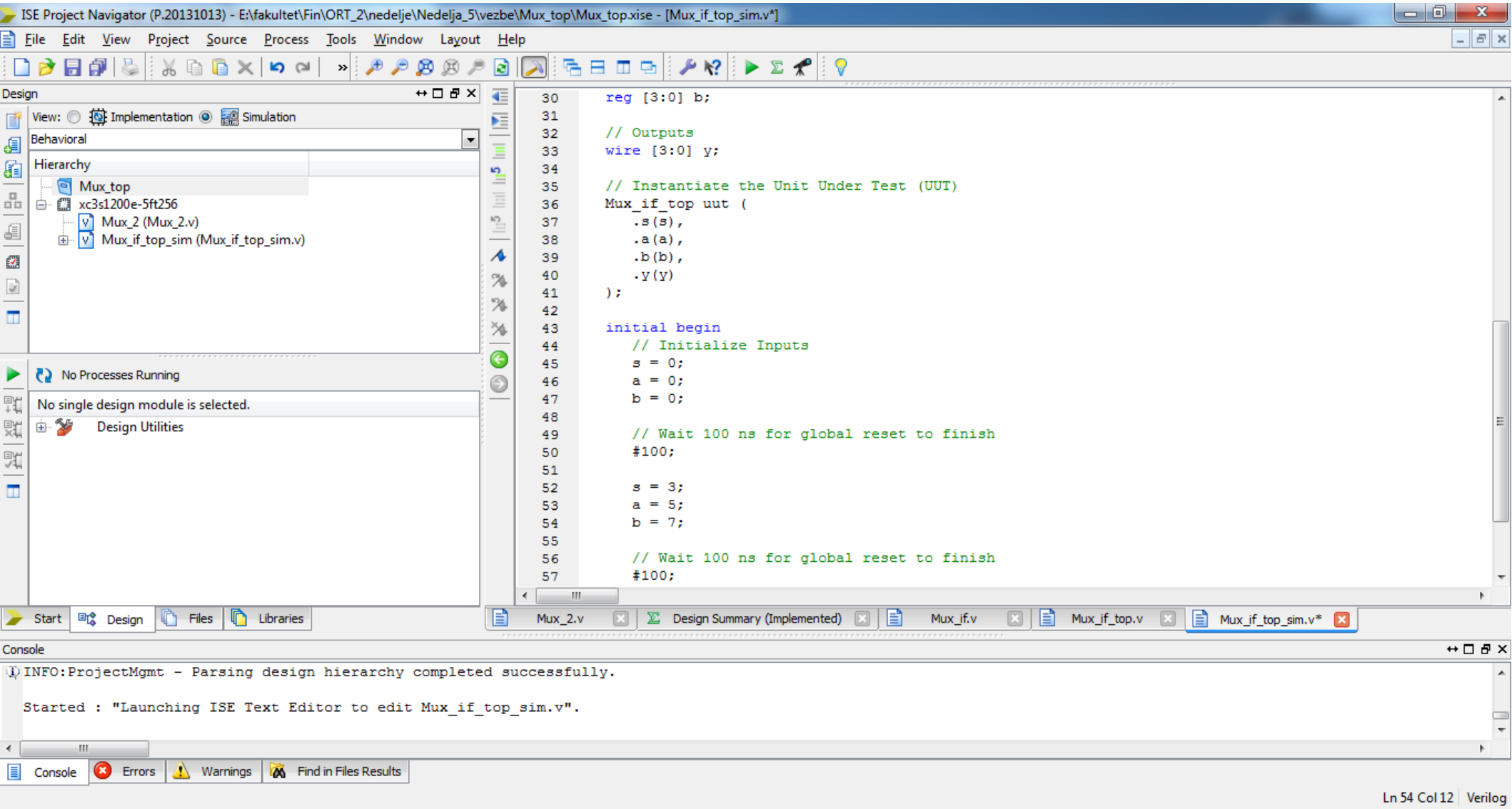
Desni klik, Set as Top Module
Klik na Implement Top Module, zelena strelica

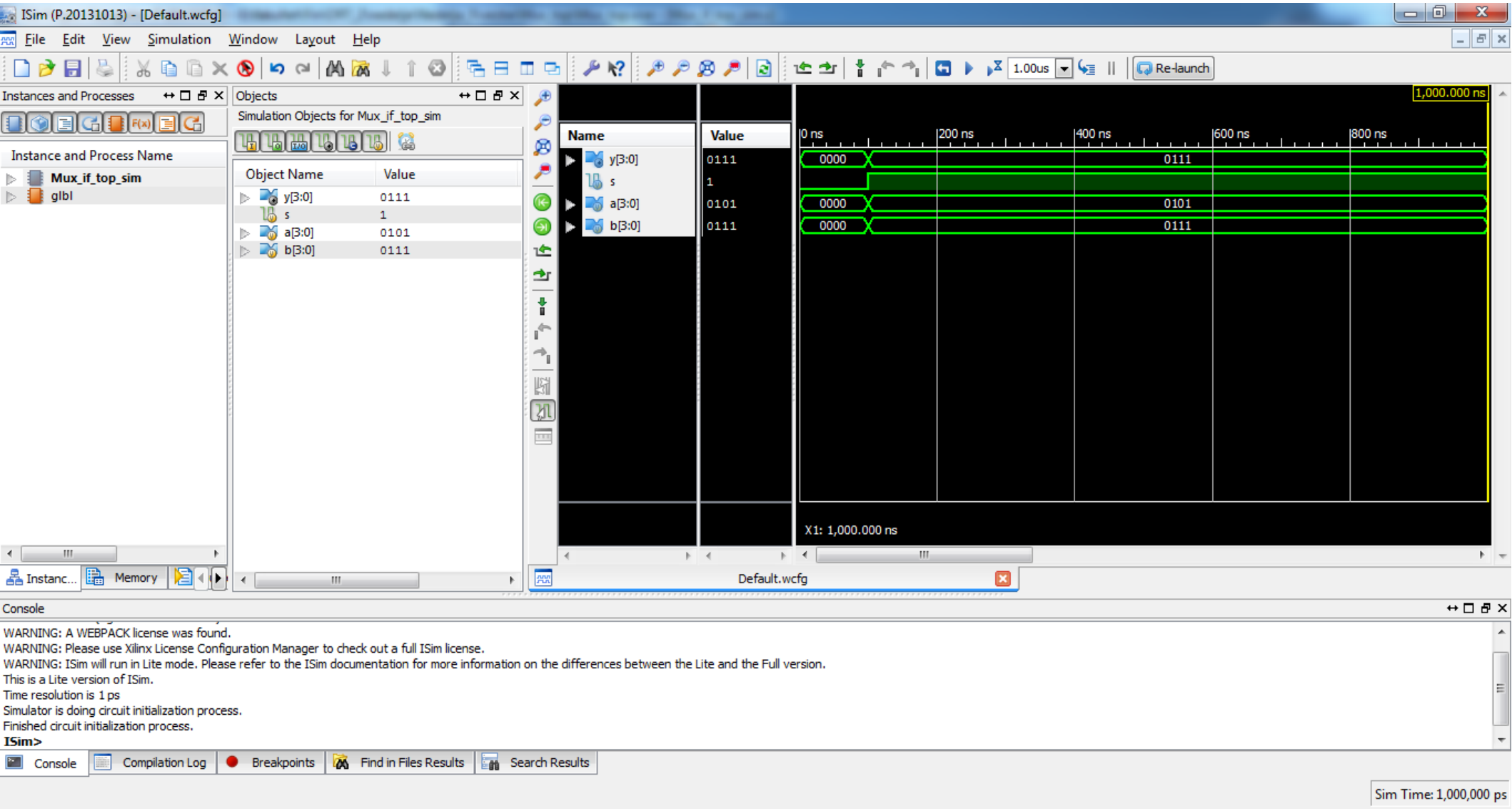
```
module Mux_if_top(
input wire s,
input wire [3:0] a,
input wire [3:0] b,
output wire [3:0] y
);

Mux_if U1
( .a(a[3]),
.b(b[3]),
.s(s),
.y(y[3])
);
Mux_if U2
( .a(a[2]),
.b(b[2]),
.s(s),
.y(y[2])
);
```

```
Mux_if U3
( .a(a[1]),
.b(b[1]),
.s(s),
.y(y[1])
);
Mux_if U4
( .a(a[0]),
.b(b[0]),
.s(s),
.y(y[0])
);

endmodule
```


ISE Project Navigator (P.20131013) - E:\fakultet\Fin\ORT_2\nedelje\Nedelja_5\vezbe\Mux_top\Mux_top.xise - [Mux_if_top_sim.v*]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
Mux_top
xc3s1200e-5ft256
Mux_2 (Mux_2.v)
Mux_if_top_sim (Mux_if_top_sim.v)
No Processes Running
No single design module is selected.
Design Utilities
Start Design Files Libraries
30 reg [3:0] b;
31
32 // Outputs
33 wire [3:0] y;
34
35 // Instantiate the Unit Under Test (UUT)
36 Mux_if_top uut (
37 .s(s),
38 .a(a),
39 .b(b),
40 .y(y)
41);
42
43 initial begin
44 // Initialize Inputs
45 s = 0;
46 a = 0;
47 b = 0;
48
49 // Wait 100 ns for global reset to finish
50 #100;
51
52 s = 3;
53 a = 5;
54 b = 7;
55
56 // Wait 100 ns for global reset to finish
57 #100;
Mux_2.v
Design Summary (Implemented)
Mux_if.v
Mux_if_top.v
Mux_if_top_sim.v*
Console
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.
Started : "Launching ISE Text Editor to edit Mux_if_top_sim.v".
Console Errors Warnings Find in Files Results
Ln 54 Col 12 Verilog


ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
1.00us
Instances and Processes
Instance and Process Name
Mux_if_top_sim
glbl
Objects
Simulation Objects for Mux_if_top_sim
Object Name
Value
y[3:0] 0111
s 1
a[3:0] 0101
b[3:0] 0111
Name
Value
y[3:0] 0111
s 1
a[3:0] 0101
b[3:0] 0111
1,000.000 ns
0 ns
200 ns
400 ns
600 ns
800 ns
0000
0111
0000
0101
0000
0111
X1: 1,000.000 ns
Instanc...
Memory
Default.wcfg
Console
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps