

# Vivado\_start\_project

File → Project → New  
Project Type: RTL Project

Čekirati: Do not specify sources at this time (lakše je za demo)

Default Part / Boards  
Za PYNQ-Z2 je tipično: xc7z020clg400-1 (Zynq-7000)

Napomena: Za čistu simulaciju nije presudno, ali je lepo da bude tačno.

Finish

# Vivado\_start\_project

New Project ✕

**Project Type**  
Specify the type of project to create.

**RTL Project**  
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

Do not specify sources at this time

Project is an extensible Vitis platform

**Post-synthesis Project**  
You will be able to add sources, view device resources, run design analysis, planning and implementation.

Do not specify sources at this time

**I/O Planning Project**  
Do not specify design sources. You will be able to view part/package resources.

**Imported Project**  
Create a Vivado project from a Synplify Project File.

**Example Project**  
Create a new Vivado project from a predefined template.



# U filteru pronaci: xc7z020clg400-1

**New Project**

**Default Part**  
Choose a default AMD part or board for your project.

Parts | Boards

[Reset All Filters](#)

Category: All Package: All Temperature: All  
Family: All Speed: All Static power: All

Search: Q: xc7z020clg400-1 (1 match)

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	BUFGs	Gb Transceivers	GTPE2 Tri
xc7z020clg400-1	400	125	53200	106400	140	0	220	32	0	0

Back Next Finish Cancel

Ovaj čip se nalazi na razvojnoj ploči PYNQ-Z2. Za simulacione vežbe nije potrebno definisati celu ploču.



### New Project Summary

- i** A new RTL project named 'mux\_decoder' will be created.
- i** The default part and product family for the new project:  
Default Part: xc7z020clg400-1  
Family: Zynq-7000  
Package: clg400  
Speed Grade: -1

To create the project, click Finish.



Back

Next

Finish

Cancel

# Kreiramo source decoder2\_4

```
module decoder2_4(  
    input [1:0] a,  
    output reg [3:0] y  
);  
  
always @(*) begin  
    case(a)  
        2'b00: y = 4'b0001;  
        2'b01: y = 4'b0010;  
        2'b10: y = 4'b0100;  
        2'b11: y = 4'b1000;  
    endcase  
end  
  
endmodule
```

# Naredba always:

- Naredba always definiše blok koda koji se izvršava svaki put kada se promene signali navedeni u listi osetljivosti.

```
always @(lista_signala)
begin
    naredbe
end
```

# Naredba always:

```
always @(*) begin
  case(a)
    2'b00: y = 4'b0001;
    2'b01: y = 4'b0010;
    2'b10: y = 4'b0100;
    2'b11: y = 4'b1000;
  endcase
end
```

izlaz y se automatski menja kada se promeni ulaz a

Osobina	assign	always
Tip logike	kombinaciona	kombinaciona ili sekvencijalna
Tip promenljive	wire	reg
Složenost logike	jednostavna logika	složenija logika
Konstrukcije	samo operatori	if, case, petlje
Način izvršavanja	kontinuirano	kada se promeni signal u listi osetljivosti

Flow Navigator

- PROJECT MANAGER
  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
  - Run Simulation
- RTL ANALYSIS
  - Run Linter
  - Open Elaborated Design
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager

PROJECT MANAGER - dekoder

Sources

Design Sources (1)

- decoder2\_4 (decoder2\_4.v)

Constraints

Simulation Sources (1)

- sim\_1 (1)

Utility Sources

Hierarchy Libraries Compile Order

Source File Properties

decoder2\_4.v

Enabled

Location: /home/apeulic/fakultet/predmeti/Osnovne/VLSI/vezbe/V\_2/deko

Type: Verilog

General Properties

Project Summary x decoder2\_4.v x

```

1 module decoder2_4(
2     input [1:0] a,
3     output reg [3:0] y
4 );
5
6 always @(*) begin
7     case(a)
8         2'b00: y = 4'b0001;
9         2'b01: y = 4'b0010;
10        2'b10: y = 4'b0100;
11        2'b11: y = 4'b1000;
12    endcase
13 end
14
15 endmodule
    
```

Tcl Console Messages Log Reports Design Runs x

Name	Constraints	Status	WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	Methodology	RQA Score	QoR Suggestions	LUT	FF	BRAM	URAM
synth_1	constrs_1	Not started															
impl_1	constrs_1	Not started															

Kreiramo sim fajl:decoder2\_4\_tb.v

# Otvorimo decoder2\_4\_tb, brisemo sve I unesemo code:

```
module decoder2_4_tb;
```

```
    reg [1:0] a;  
    wire [3:0] y;
```

```
    decoder2_4 uut (  
        .a(a),  
        .y(y)  
    );
```

```
    initial begin  
        a = 2'b00;  
        #10 a = 2'b01;  
        #10 a = 2'b10;  
        #10 a = 2'b11;  
        #10 $finish;  
    end
```

```
endmodule
```

## Flow Navigator

## PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
  - Run Simulation
- RTL ANALYSIS
  - Run Linter
  - Open Elaborated Design
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager

## PROJECT MANAGER - Dekoder

## Sources

Design Sources (1)

- decoder2\_4 (decoder2\_4.v)

Constraints

Simulation Sources (1)

- sim\_1 (1)
  - decoder2\_4\_tb (decoder2\_4\_tb.v) (1)

Hierarchy Libraries Compile Order

## Source File Properties

decoder2\_4\_tb.v

Enabled

Location: /home/apeulic/fakultet/predmeti/Osnovne/VLSI/vezbe/V\_2/Deko

Type: Verilog

General Properties

## Project Summary

## decoder2\_4.v

## decoder2\_4\_tb.v

```

/home/apeulic/fakultet/predmeti/Osnovne/VLSI/vezbe/V_2/Dekoder/Dekoder.srcs/sim_1/new/decoder2_4_tb.v
1 module decoder2_4_tb;
2
3   reg [1:0] a;
4   wire [3:0] y;
5
6   decoder2_4 uut (
7       .a(a),
8       .y(y)
9   );
10
11 initial begin
12     a = 2'b00;
13     #10 a = 2'b01;
14     #10 a = 2'b10;
15     #10 a = 2'b11;
16     #10 $finish;
17 end
18
19 endmodule

```

## Tcl Console

## Messages

## Log

## Reports

## Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	Methodology	RQA Score	QoR Suggestions	LUT	FF	BRAM	URAM
synth_1	constrs_1	Not started															
impl_1	constrs_1	Not started															

Flow Navigator

- PROJECT MANAGER
  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION**
  - Run Simulation
- RTL ANALYSIS
  - Run Linter
  - Open Elaborated Design
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager

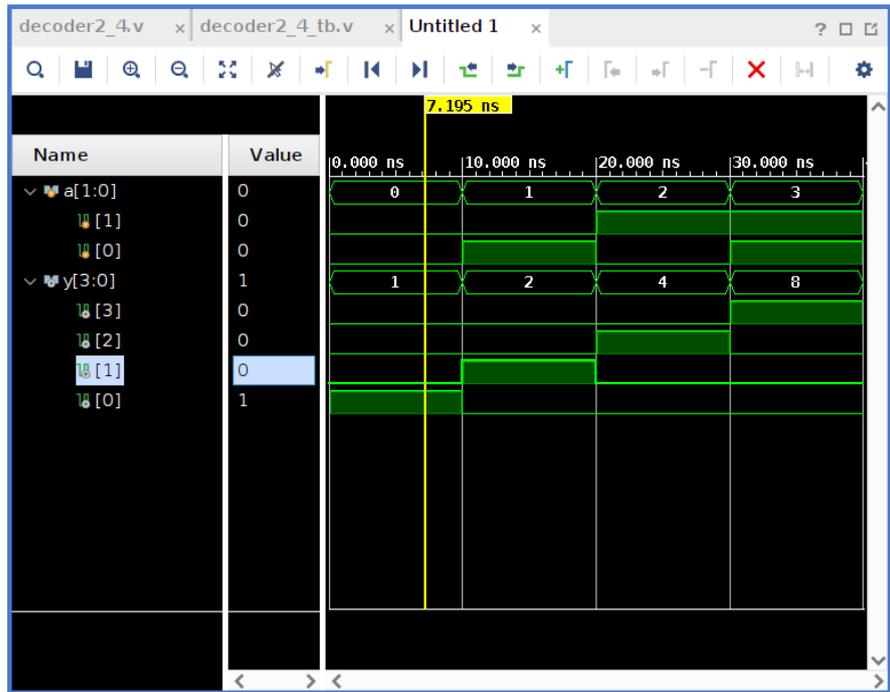
SIMULATION - Behavioral Simulation - Functional - sim\_1 - decoder2\_4\_tb

Scope Sources

Name	Design Unit	Blk
decoder2_4_tb	decoder2_4_tb	Ve
uut	decoder2_4	Ve
gbl	gbl	Ve

Objects Protocol Inst

Name	Value	Data Type
a[1:0]	3	Array
y[3:0]	8	Array



Tcl Console Messages Log

```

$finish called at time : 40 ns : File "/home/apeulic/fakultet/predmeti/Osnovne/VLSI/vezbe/V_2/Dekoder/Dekoder.srscs/sim_1/new/decoder2_4_tb.v" Line 16
xsim: Time (s): cpu = 00:00:10 ; elapsed = 00:00:06 . Memory (MB): peak = 10304.234 ; gain = 91.523 ; free physical = 3853 ; free virtual = 11256
INFO: [USF-XSim-96] XSim completed. Design snapshot 'decoder2_4_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:20 ; elapsed = 00:00:16 . Memory (MB): peak = 10304.234 ; gain = 92.930 ; free physical = 3853 ; free virtual = 11257
    
```

Type a Tcl command here