STM32 Cortex M3- M4 IO portovi

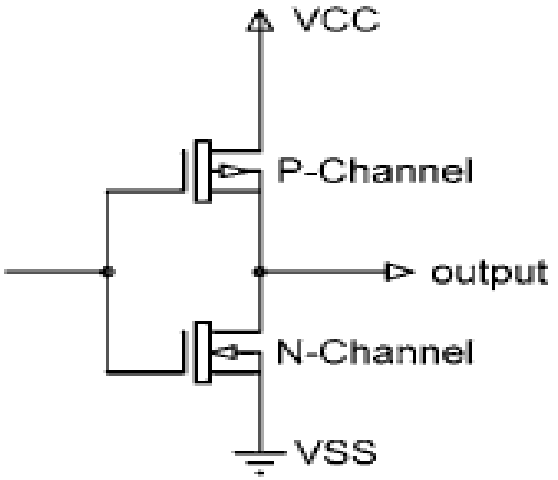


Figure 2.5: Push-pull output pin.

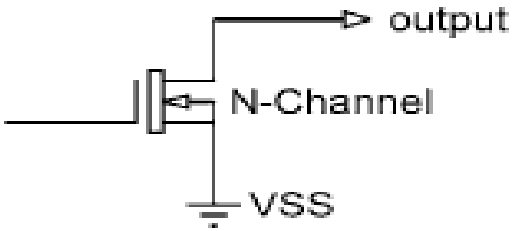


Figure 2.6: Open-drain output pin.

STM32 Cortex M3- M4 IO portovi

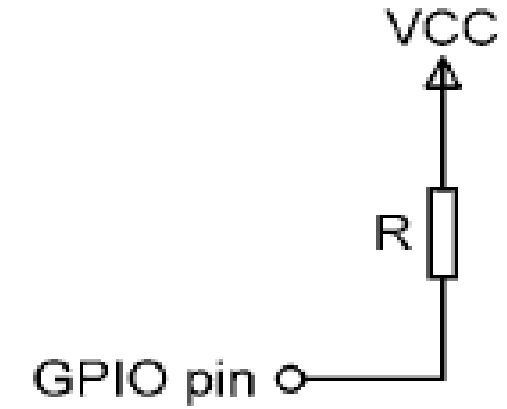


Figure 2.7: Pull-up pin.

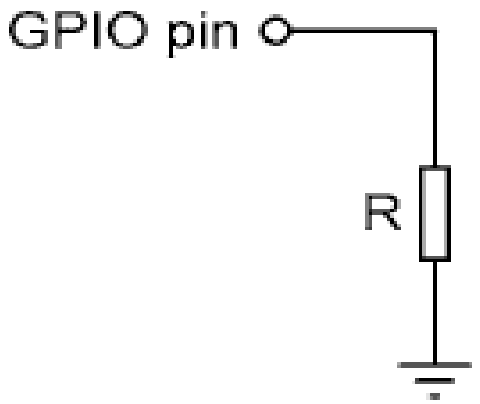


Figure 2.8: Pull-down pin.

STM32 Cortex M3- M4 IO portovi

- Registri podataka porta GPIOx_IDR i GPIOx_ODR se koriste za čitanje i pisanje podataka na port, respektivno.
- Kada je pin konfigurisan kao izlaz, vrednost upisana u registar izlaznih podataka GPIOx_ODR izlazi na I/O pin.
- Moguće je koristiti izlazni drajver u push-pull režimu ili režimu open drain (pokreće se samo niski nivo, visoki nivo je HI-Z).
- Registar ulaznih podataka GPIOx_IDR hvata podatke prisutne na I/O pinu na svakom ciklusu AHB takta.

STM32 Cortex M3- M4 IO portovi

Address offset: 0x10

Reset value: 0x0000 XXXX (where X means undefined)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bits 31:16 Reserved, must be kept at reset value.

Bits 15:0 **IDy:** Port input data bit (y = 0..15)
These bits are read-only. They contain the input value of the corresponding I/O port.

Figure 2.10: GPIOx_IDR port input register.

STM32 Cortex M3- M4 IO portovi

Address offset: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OD15	OD14	OD13	OD12	OD11	OD10	OD9	OD8	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:16 Reserved, must be kept at reset value.

Bits 15:0 **ODy:** Port output data bit (y = 0..15)

These bits can be read and written by software.

Note: For atomic bit set/reset, the OD bits can be individually set and/or reset by writing to the GPIOx_BSRR or GPIOx_BRR registers (x = A..F).

Figure 2.11: GPIOx_ODR port output register.

STM32 Cortex M3- M4 IO portovi

All GPIO pins have weak internal pull-up and pull-down resistors, which can be activated or not depending on the value in the GPIOx_PUPDR register (Figure 2.12).

Address offset: 0x0C

Reset values:

- 0x6400 0000 for port A
- 0x0000 0100 for port B
- 0x0000 0000 for other ports

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PUPD15[1:0]		PUPD14[1:0]		PUPD13[1:0]		PUPD12[1:0]		PUPD11[1:0]		PUPD10[1:0]		PUPD9[1:0]		PUPD8[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PUPD7[1:0]		PUPD6[1:0]		PUPD5[1:0]		PUPD4[1:0]		PUPD3[1:0]		PUPD2[1:0]		PUPD1[1:0]		PUPD0[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

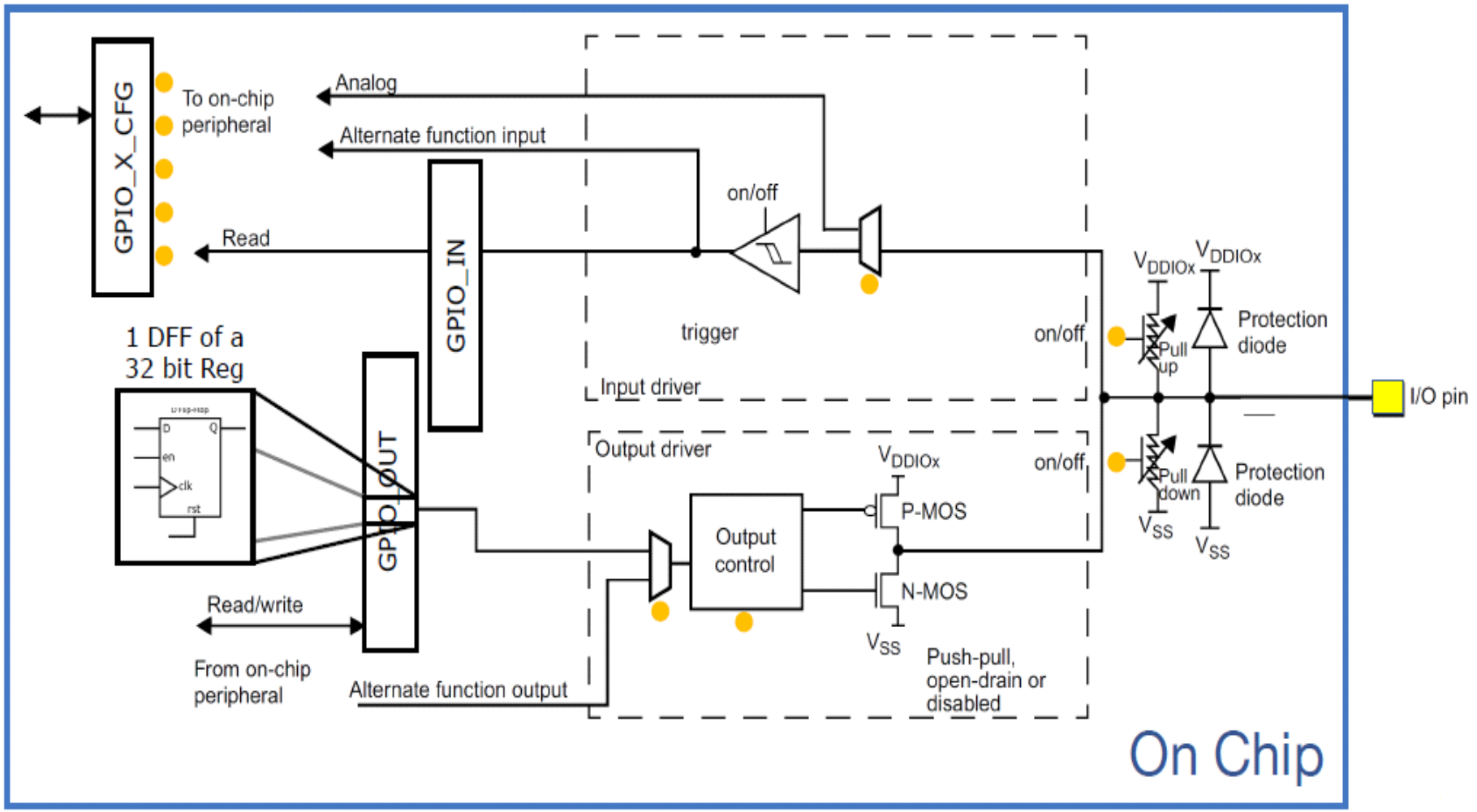
Bits 2y+1:2y **PUPDy[1:0]**: Port x configuration bits (y = 0..15)

These bits are written by software to configure the I/O pull-up or pull-down

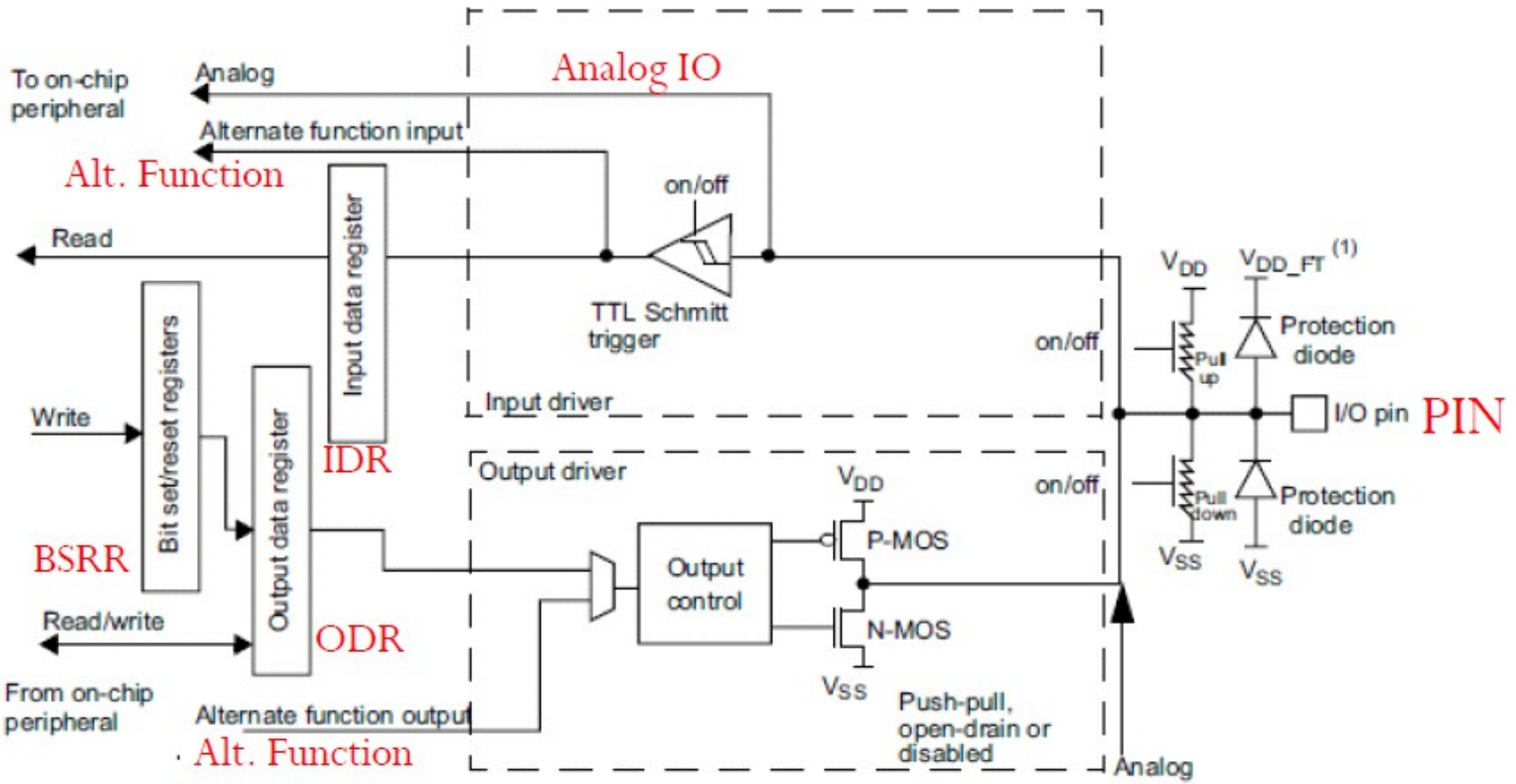
00: No pull-up, pull-down
01: Pull-up
10: Pull-down
11: Reserved

Figure 2.12: GPIOx_PUPDR pull-up/pull-down register.

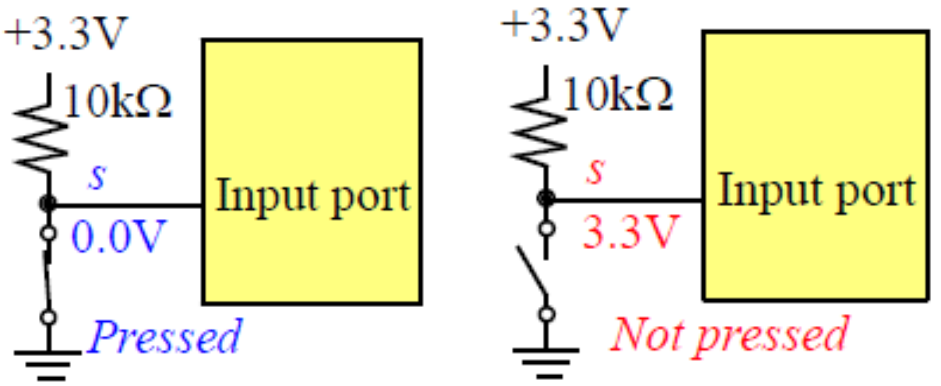
STM32 Cortex M3- M4 IO portovi



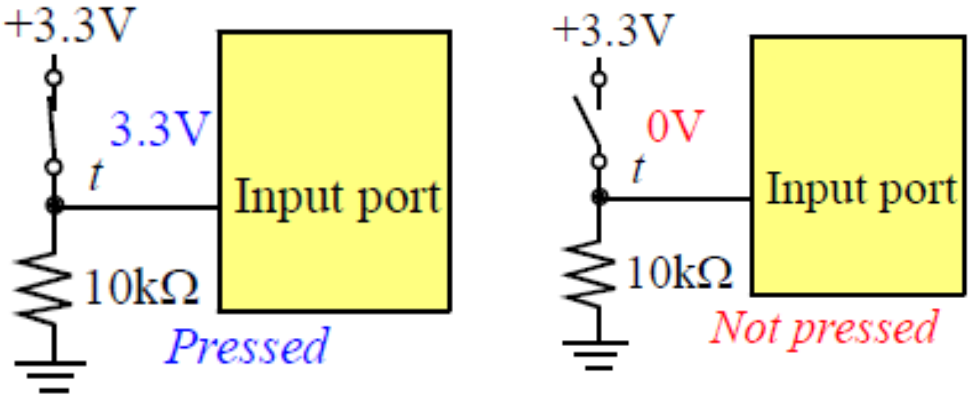
STM32 Cortex M3- M4 IO portovi

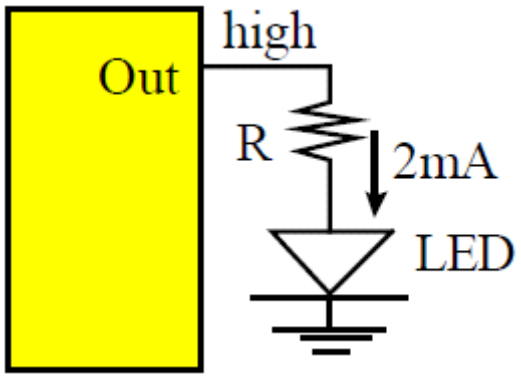


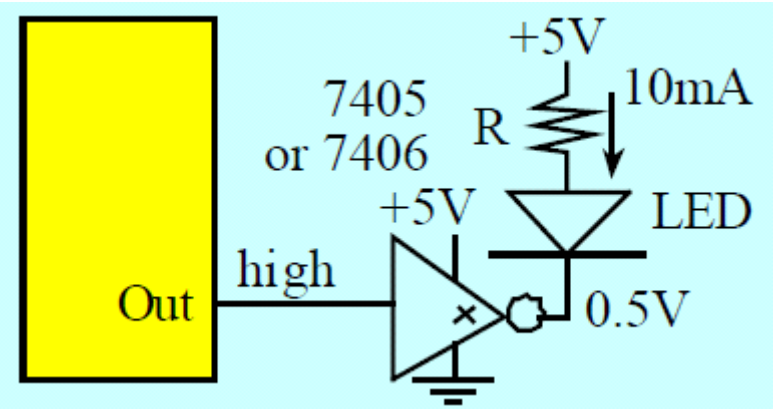
- Негативна логика:
  - Притистнут прекидач – 0V false
  - Непритистнут прекидач – 3,3V true

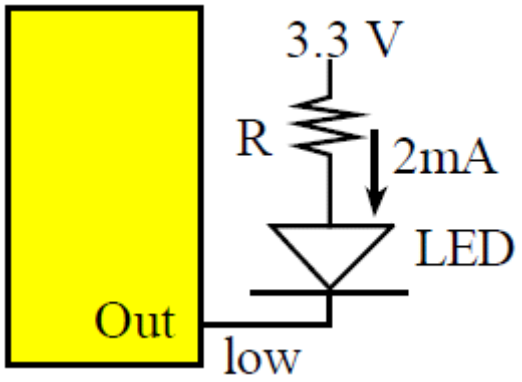


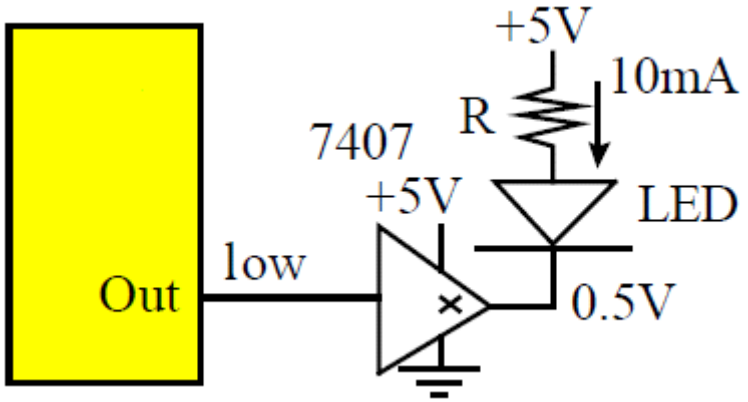
- Позитивна логика:
  - Притистнут прекидач – 3,3V true
  - Непритистнут прекидач – 0V false




Out
high
R
2mA
LED


+5V
7405
or 7406
R
10mA
+5V
LED
Out
high
0.5V


3.3 V
R
2mA
LED
Out
low


+5V
10mA
R
7407
+5V
LED
Out
low
0.5V