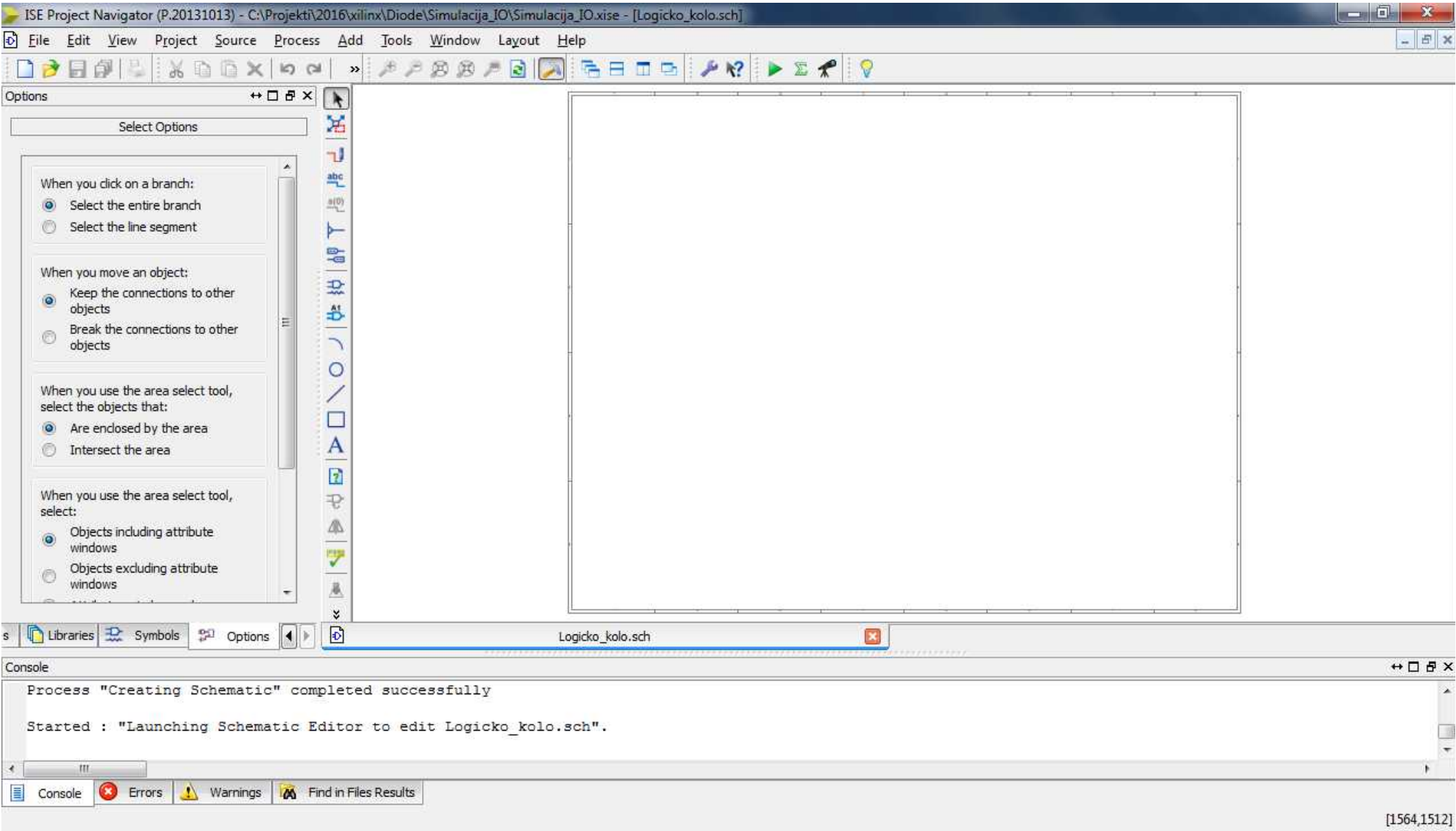
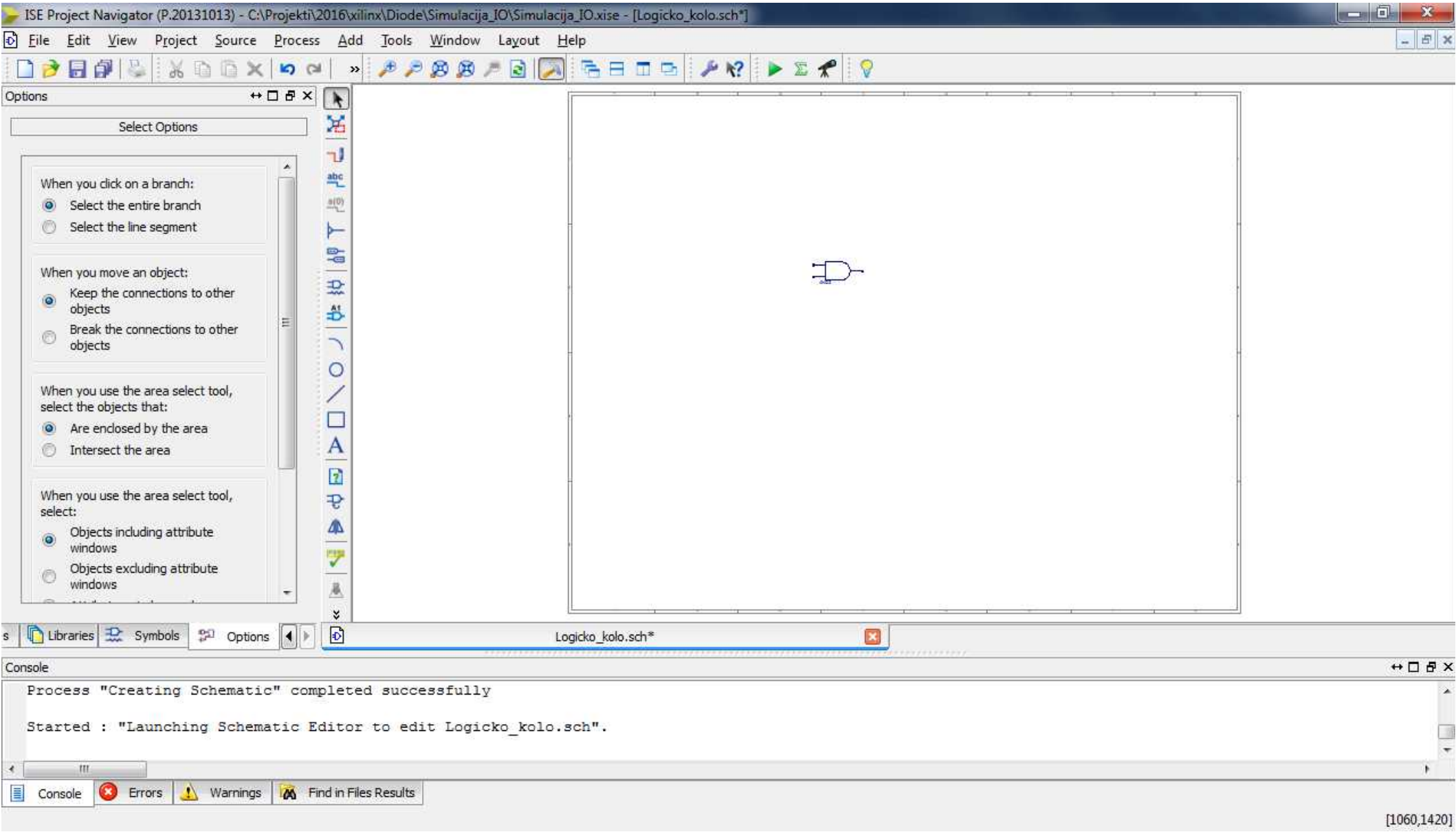
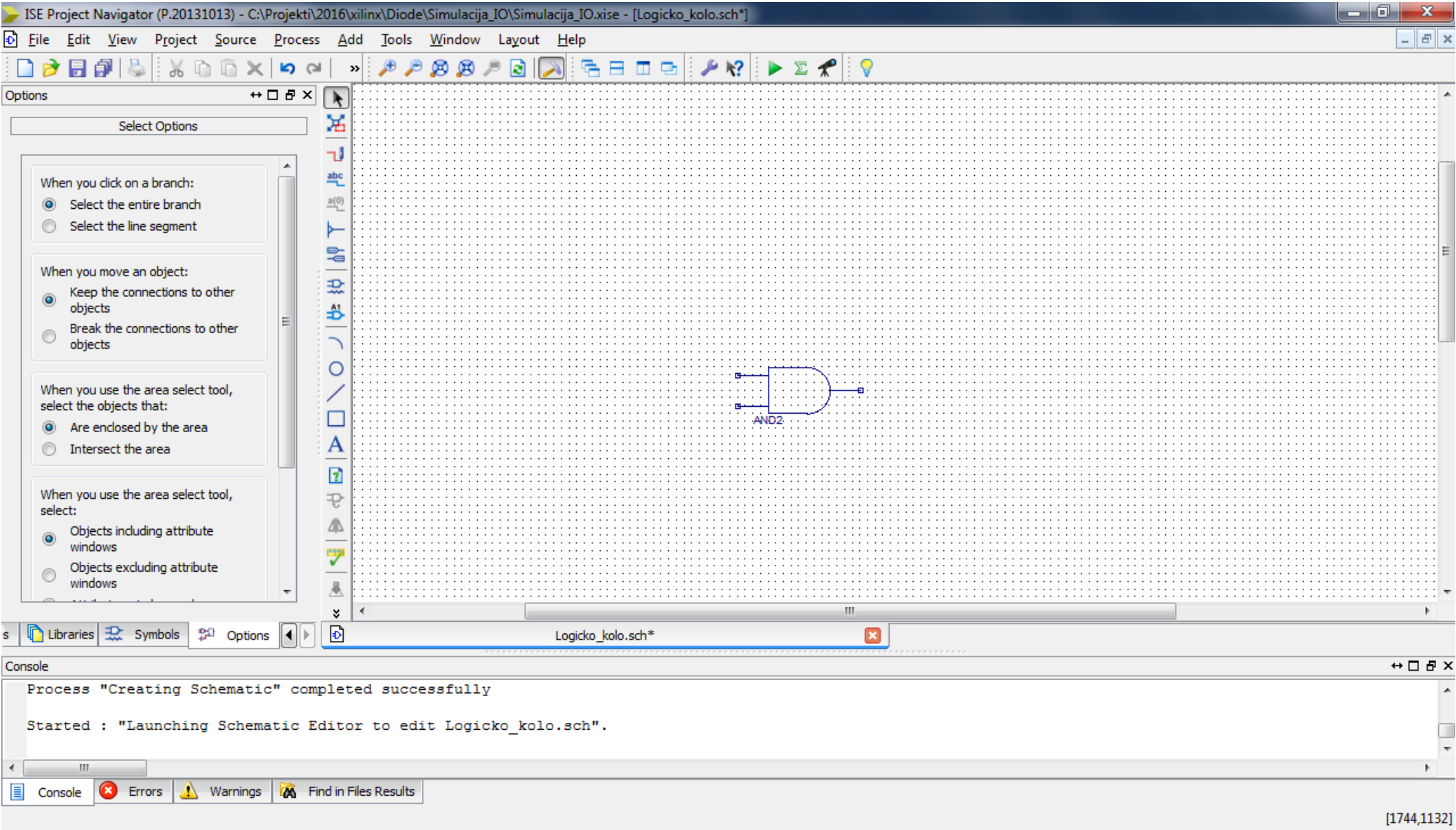
Simulacija rada logickog kola

Otvorimo novi projekata, izaberemo Schematik

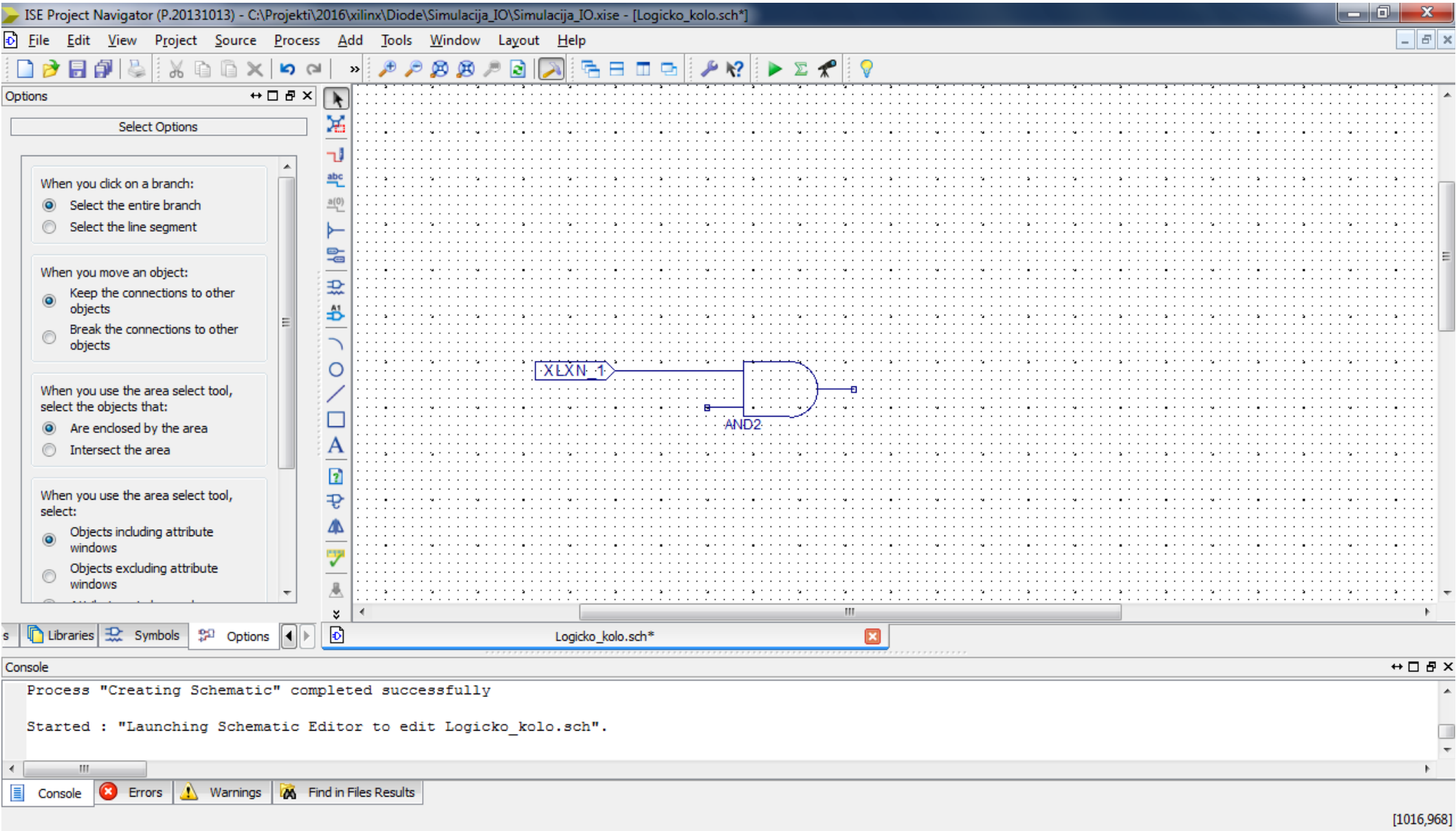


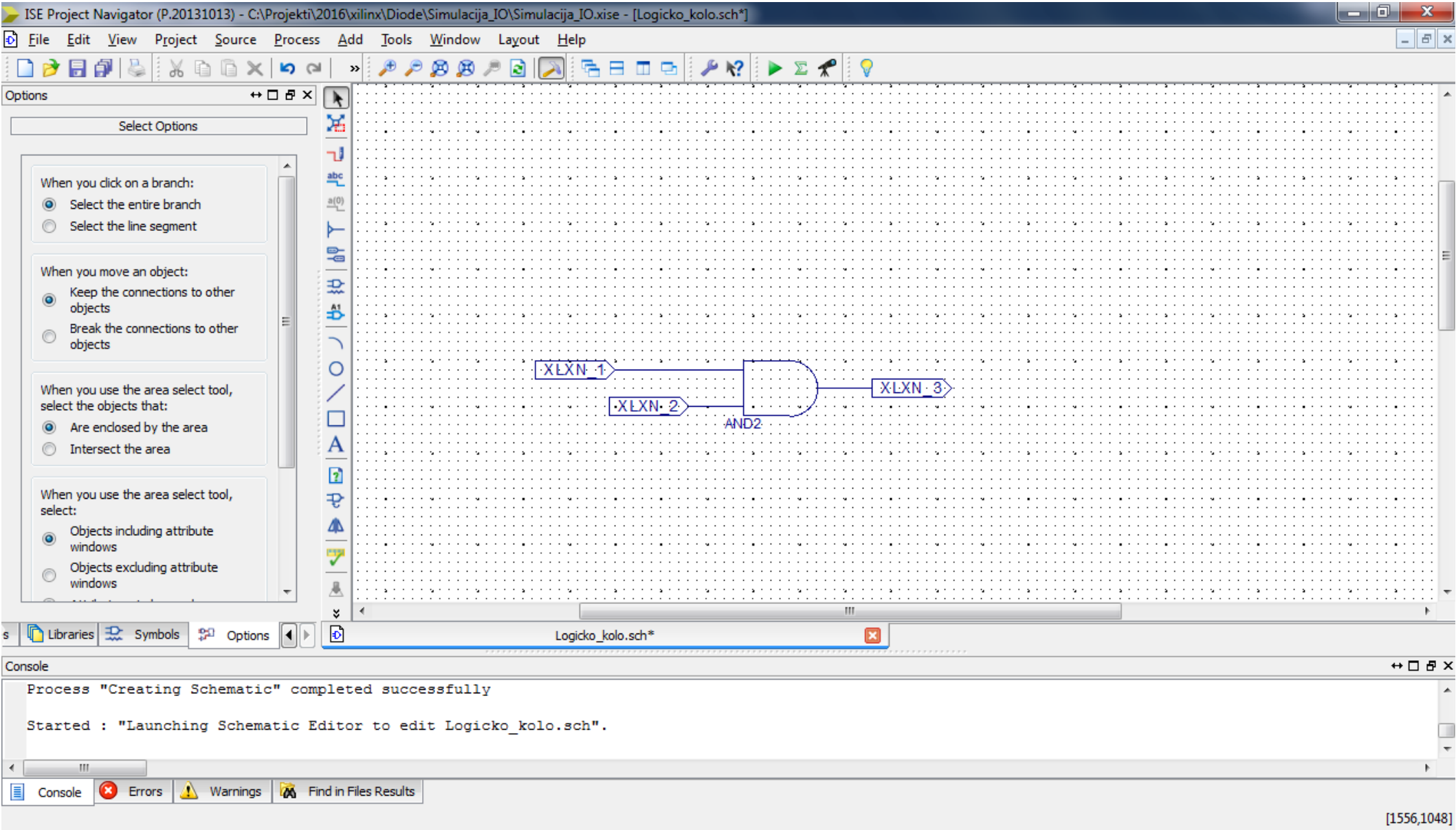
Izaberemo simulaciju jednostavnog AND kola

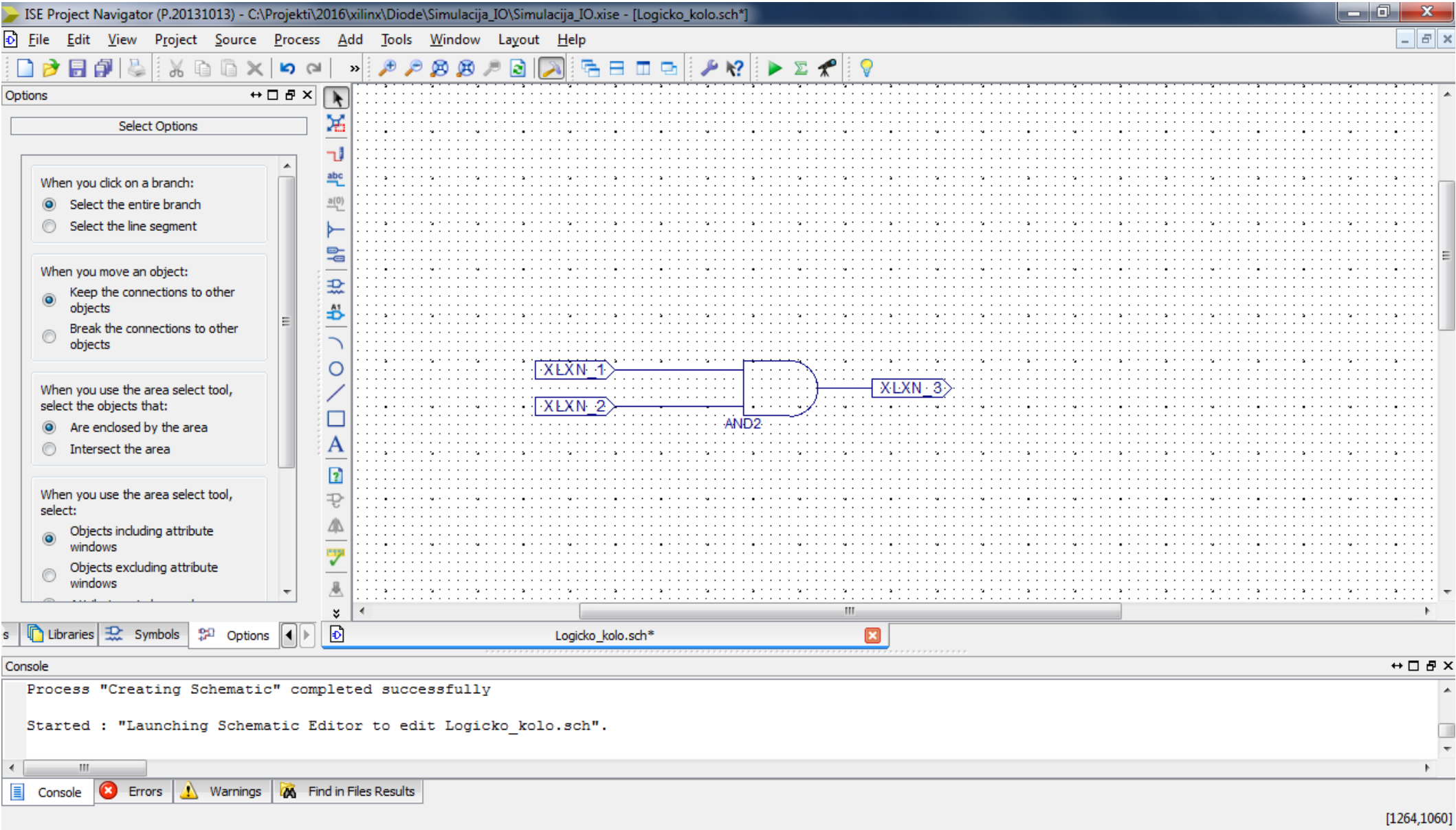



ISE Project Navigator (P.20131013) - C:\Projekti\2016\xilinx\Diode\Simulacija_IO\Simulacija_IO.xise - [Logicko_kolo.sch*]
File Edit View Project Source Process Add Tools Window Layout Help
Options
Select Options
When you click on a branch:
Select the entire branch
Select the line segment
When you move an object:
Keep the connections to other objects
Break the connections to other objects
When you use the area select tool, select the objects that:
Are enclosed by the area
Intersect the area
When you use the area select tool, select:
Objects including attribute windows
Objects excluding attribute windows
AND2
Libraries
Symbols
Options
Logicko_kolo.sch*
Console
Process "Creating Schematic" completed successfully
Started : "Launching Schematic Editor to edit Logicko_kolo.sch".
Console
Errors
Warnings
Find in Files Results
[1744,1132]

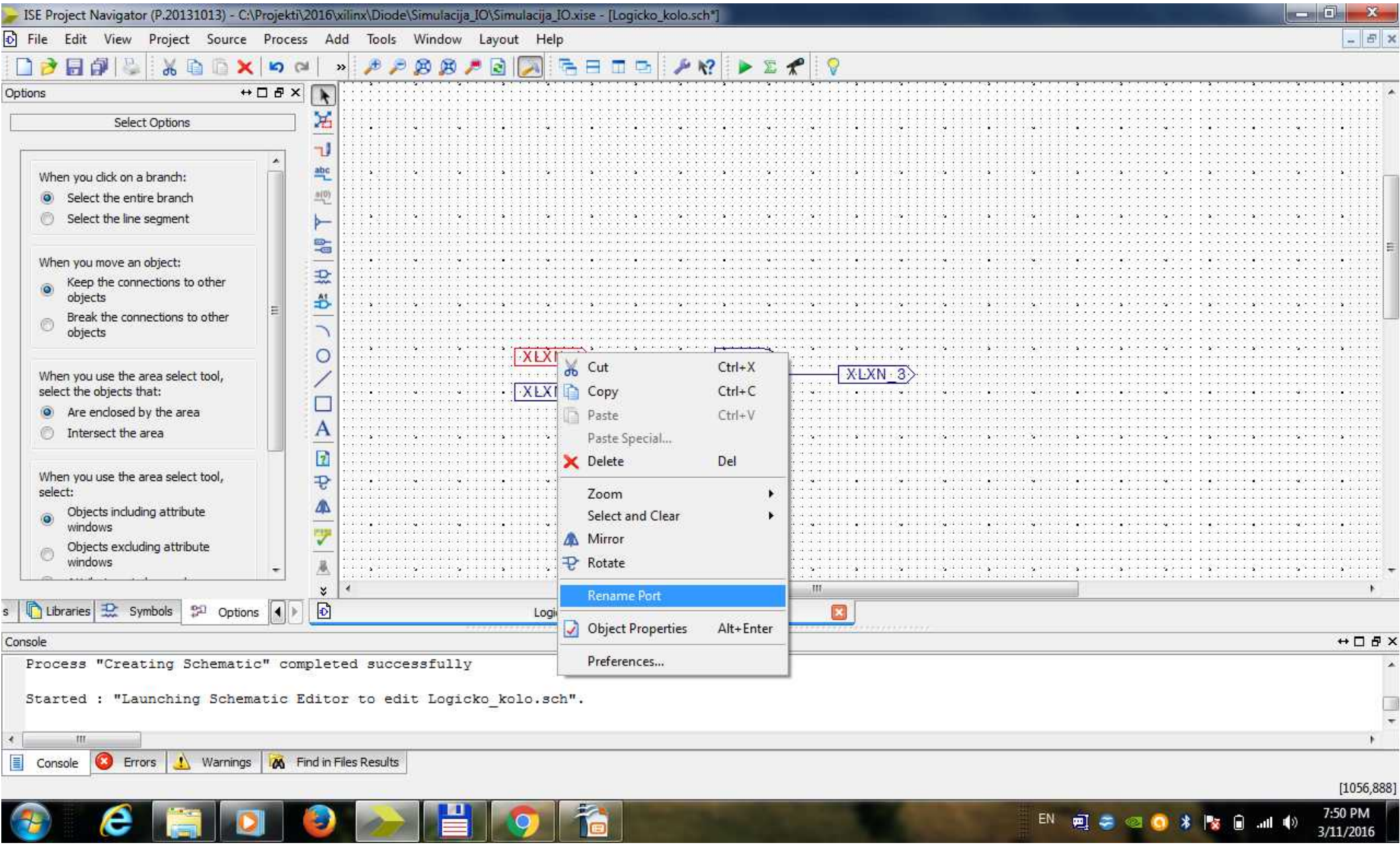
Dodamo ulaze I izlaz

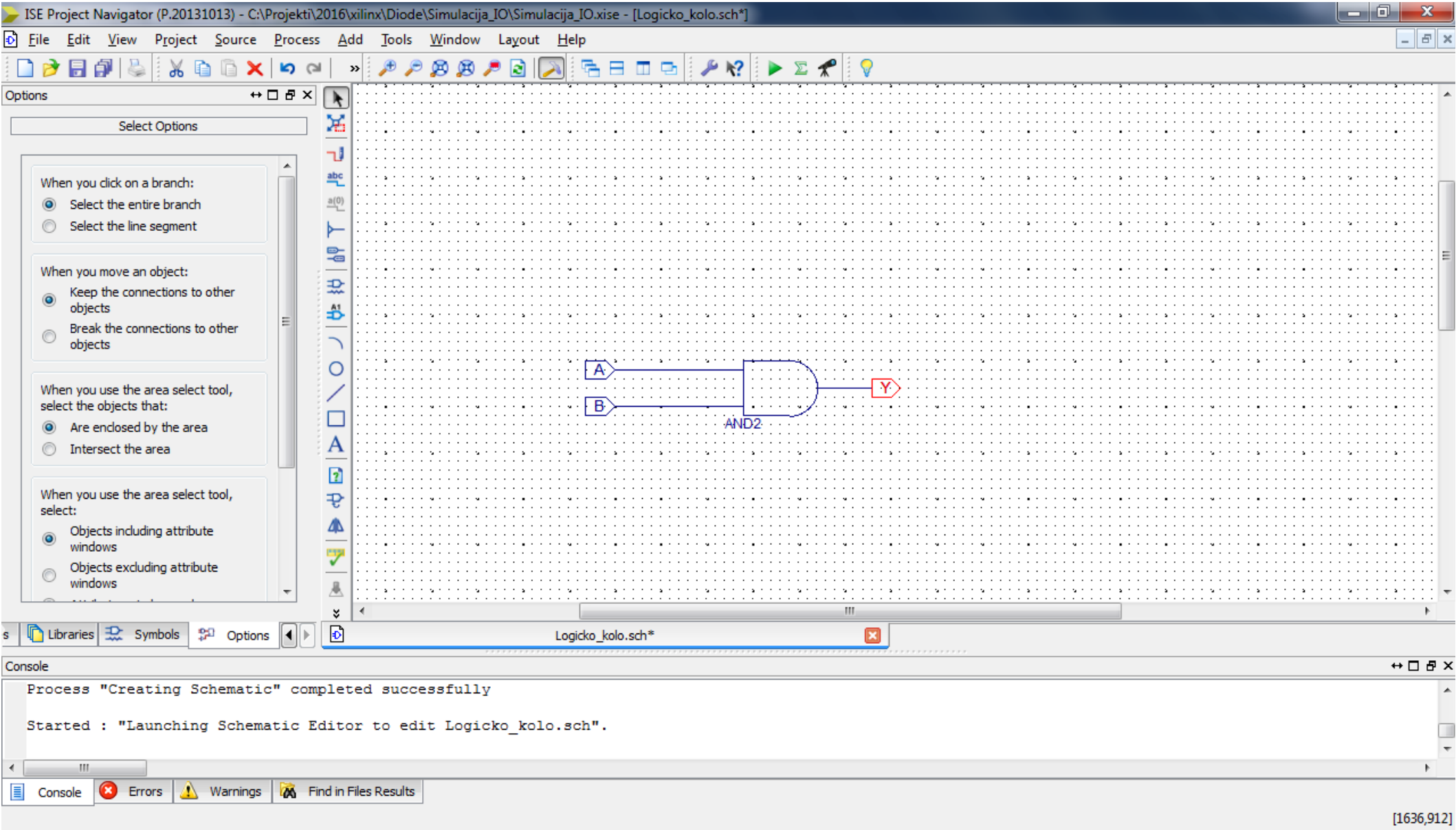



ISE Project Navigator (P.20131013) - C:\Projekti\2016\xilinx\Diode\Simulacija_IO\Simulacija_IO.xise - [Logicko_kolo.sch*]
File Edit View Project Source Process Add Tools Window Layout Help
Options
Select Options
When you click on a branch:
Select the entire branch
Select the line segment
When you move an object:
Keep the connections to other objects
Break the connections to other objects
When you use the area select tool, select the objects that:
Are enclosed by the area
Intersect the area
When you use the area select tool, select:
Objects including attribute windows
Objects excluding attribute windows
XLXN_1
XLXN_2
AND2
XLXN_3
Libraries
Symbols
Options
Logicko_kolo.sch*
Console
Process "Creating Schematic" completed successfully
Started : "Launching Schematic Editor to edit Logicko_kolo.sch".
Console
Errors
Warnings
Find in Files Results
[1556,1048]

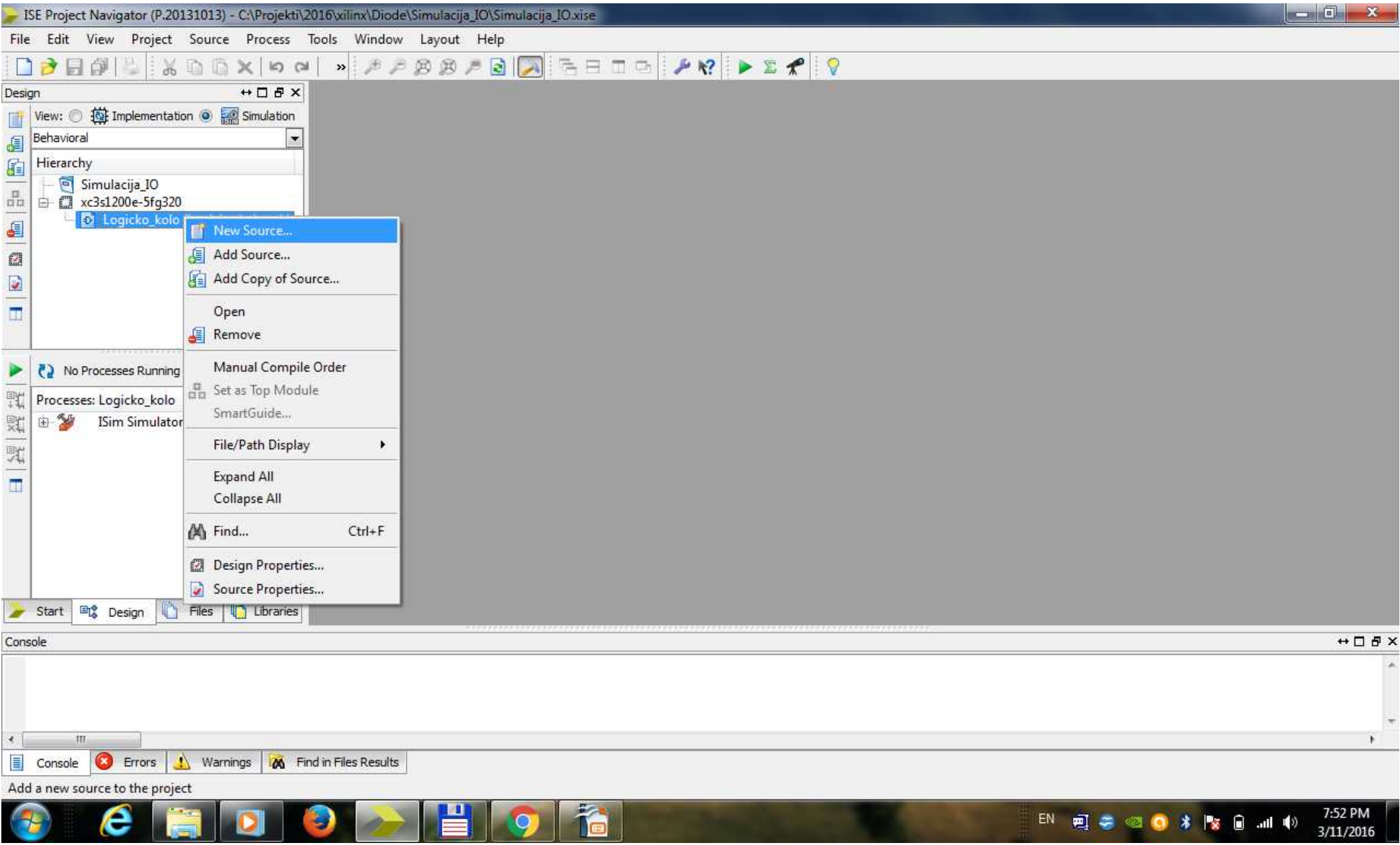

ISE Project Navigator (P.20131013) - C:\Projekti\2016\xilinx\Diode\Simulacija_IO\Simulacija_IO.xise - [Logicko_kolo.sch*]
File Edit View Project Source Process Add Tools Window Layout Help
Options
Select Options
When you click on a branch:
Select the entire branch
Select the line segment
When you move an object:
Keep the connections to other objects
Break the connections to other objects
When you use the area select tool, select the objects that:
Are enclosed by the area
Intersect the area
When you use the area select tool, select:
Objects including attribute windows
Objects excluding attribute windows
XLXN_1
XLXN_2
AND2
XLXN_3
Libraries
Symbols
Options
Logicko_kolo.sch*
Console
Process "Creating Schematic" completed successfully
Started : "Launching Schematic Editor to edit Logicko_kolo.sch".
Console
Errors
Warnings
Find in Files Results
[1264,1060]

Desni klik na IO, izaberemo Rename I ulazima dodelimo ime A I B, a izlazu Y

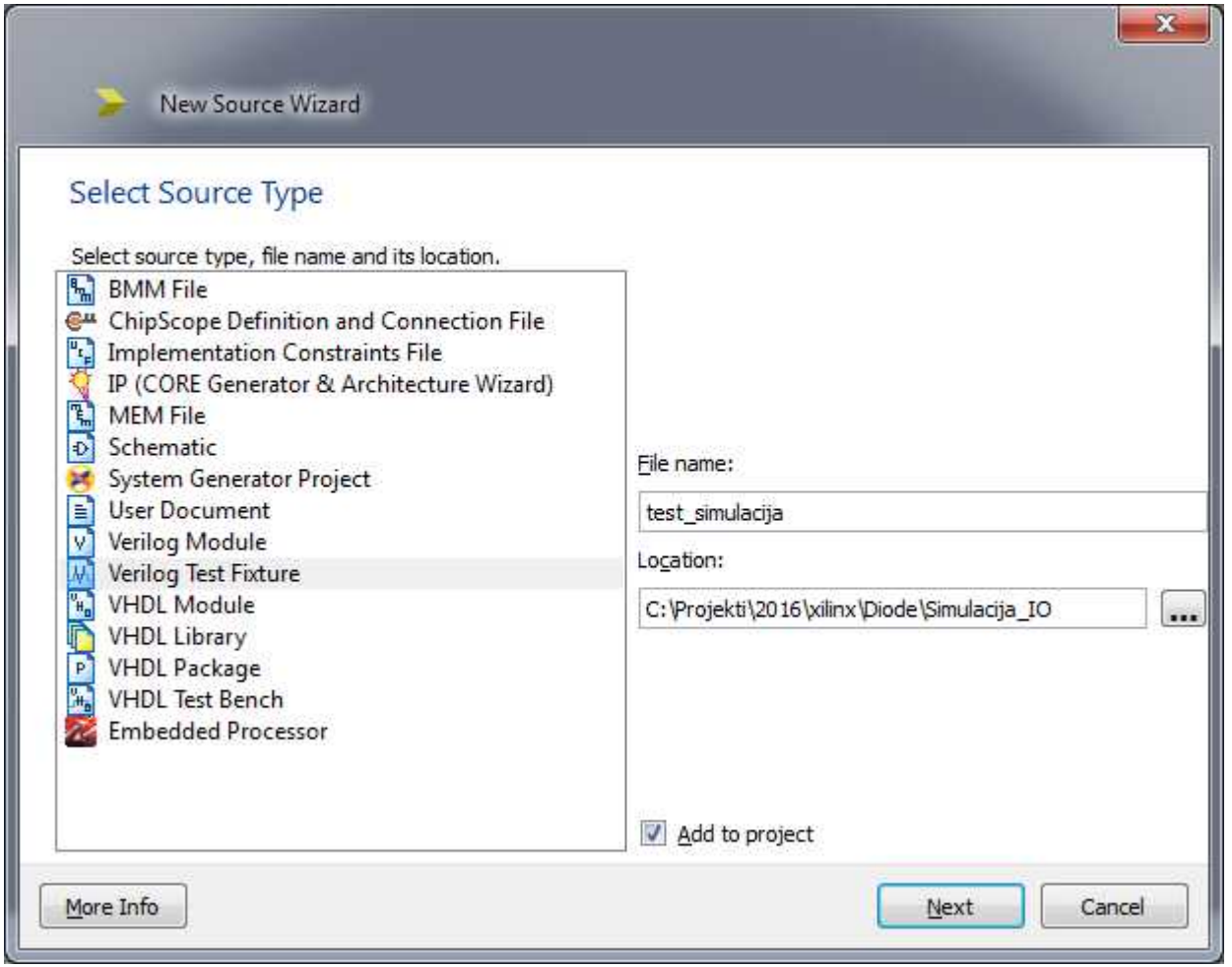



ISE Project Navigator (P.20131013) - C:\Projekti\2016\xilinx\Diode\Simulacija_IO\Simulacija_IO.xise - [Logicko_kolo.sch*]
File Edit View Project Source Process Add Tools Window Layout Help
Options
Select Options
When you click on a branch:
Select the entire branch
Select the line segment
When you move an object:
Keep the connections to other objects
Break the connections to other objects
When you use the area select tool, select the objects that:
Are enclosed by the area
Intersect the area
When you use the area select tool, select:
Objects including attribute windows
Objects excluding attribute windows
A
B
Y
AND2
Libraries
Symbols
Options
Logicko_kolo.sch*
Console
Process "Creating Schematic" completed successfully
Started : "Launching Schematic Editor to edit Logicko_kolo.sch".
Console
Errors
Warnings
Find in Files Results
[1636,912]

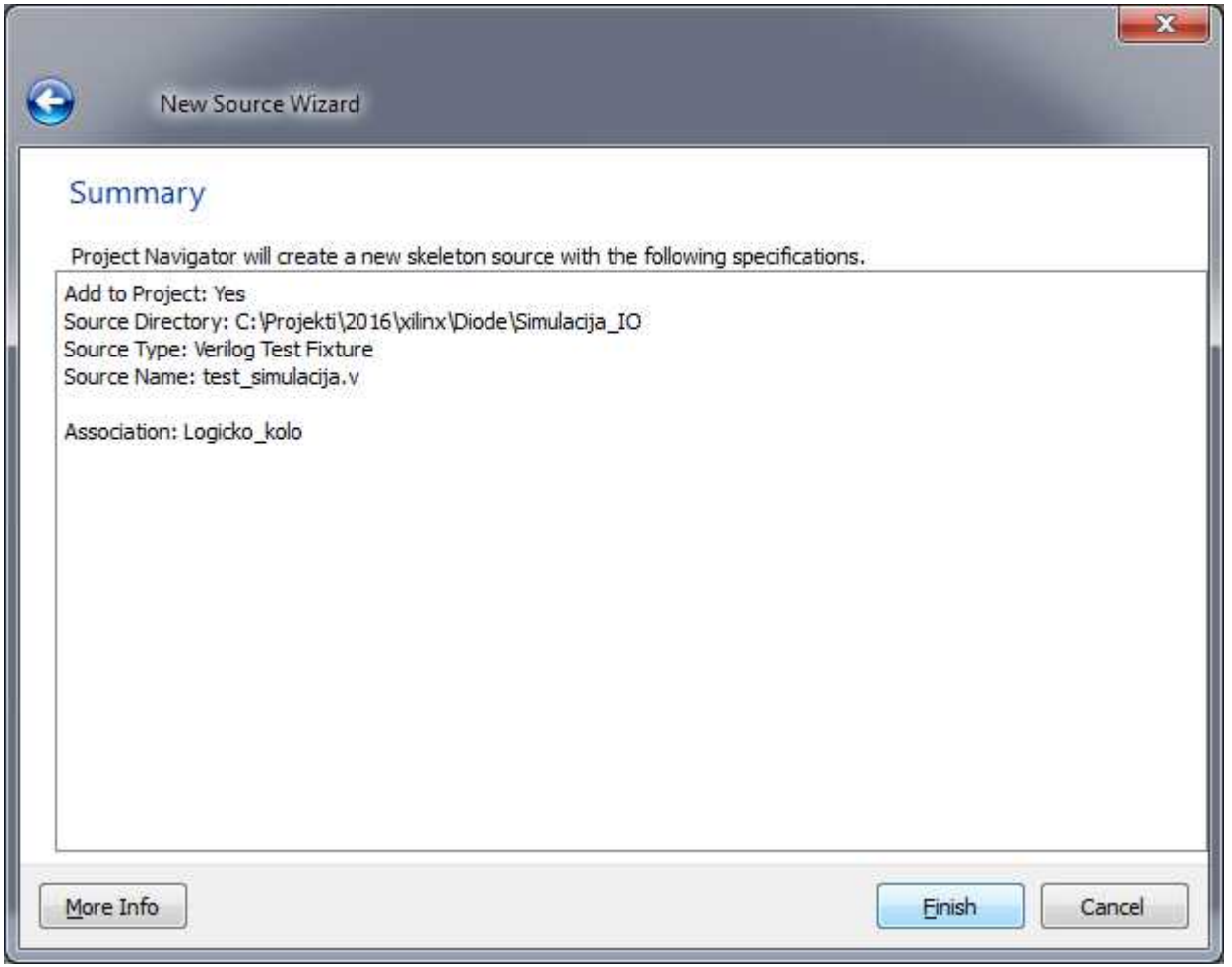
Klik na logicko kolo, pa New Source...



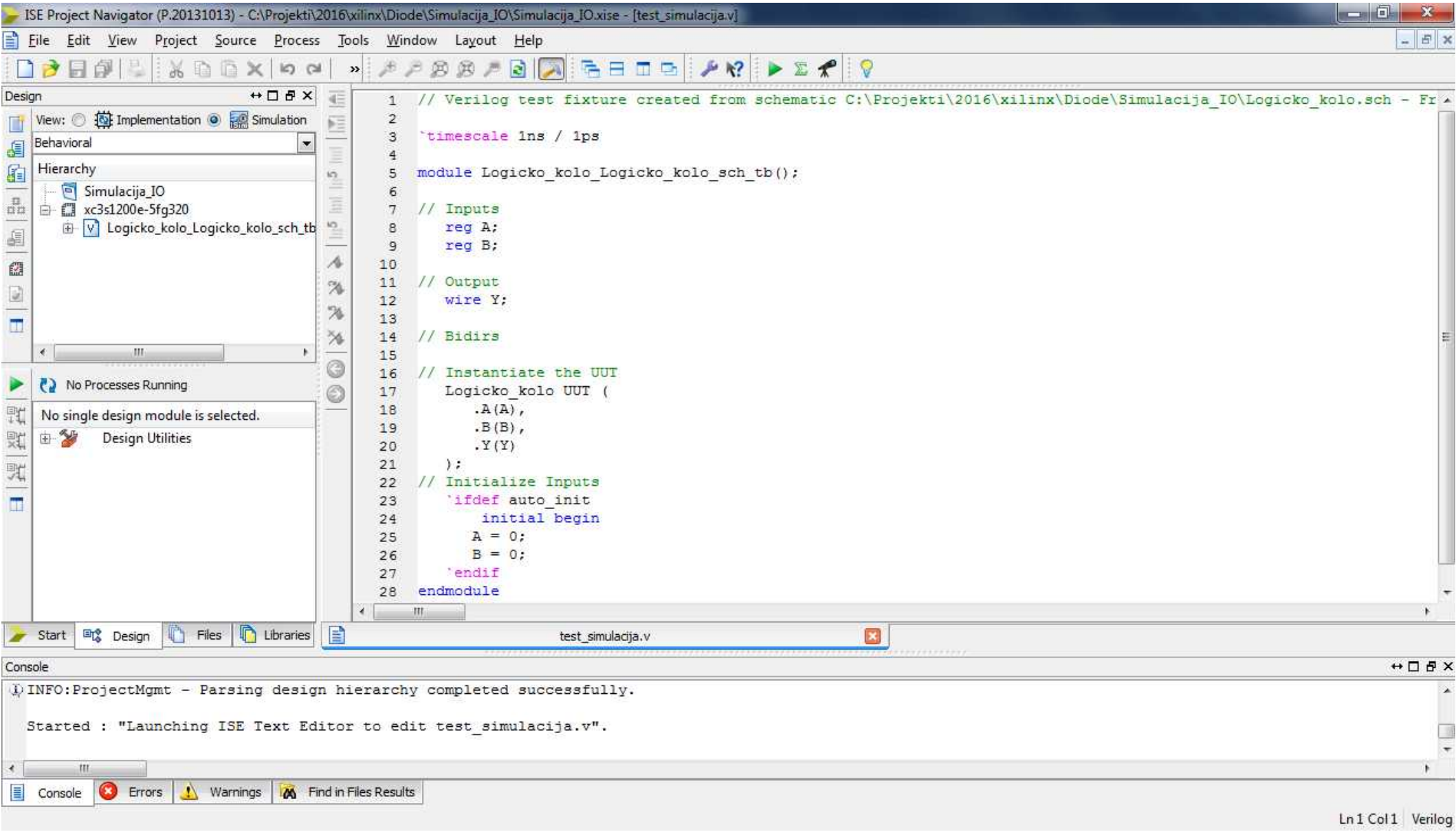
Selektujemo Verilog Test Fixture, dodlimo ime na primer test_simulacija



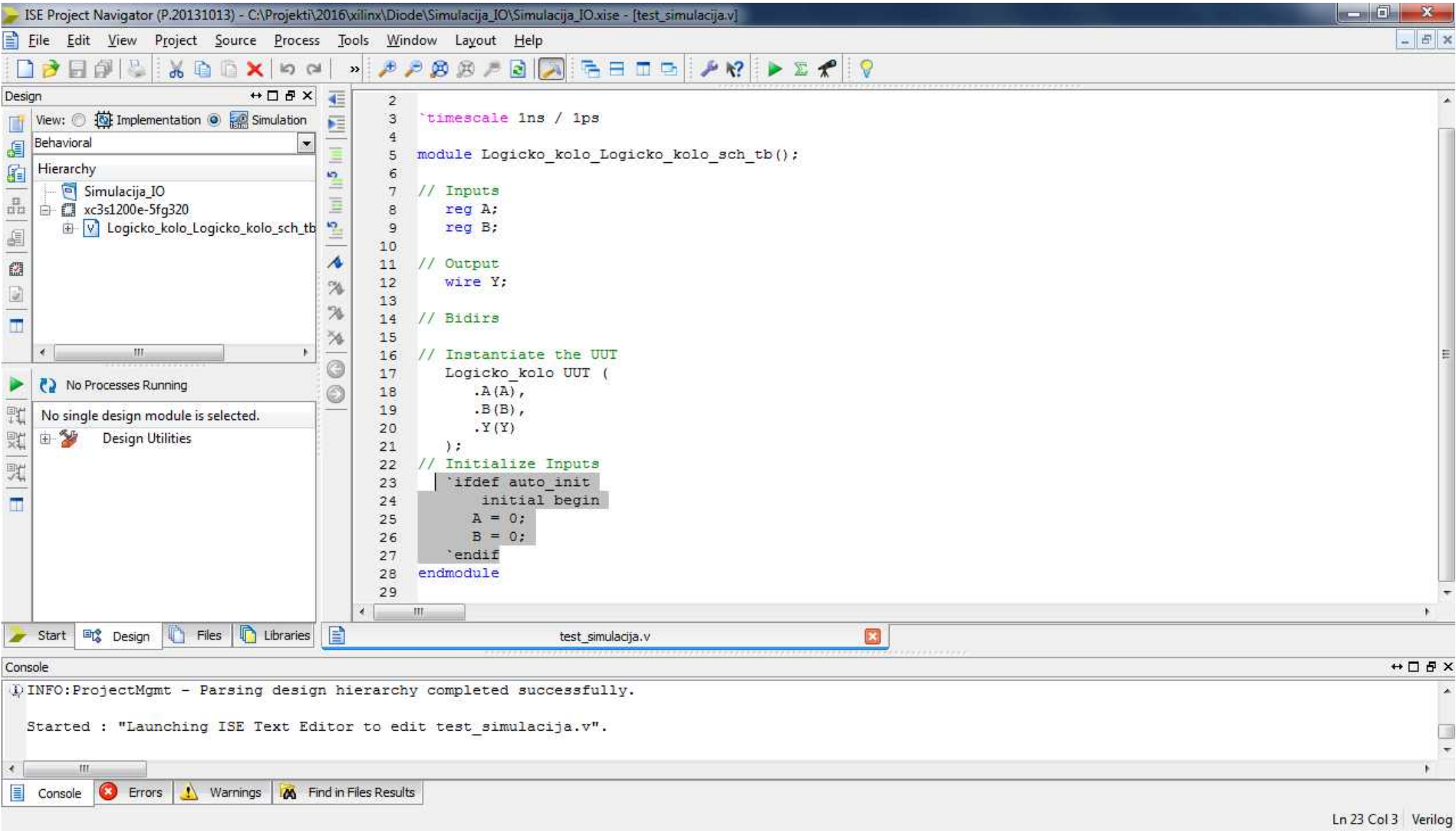
Klik na Finish



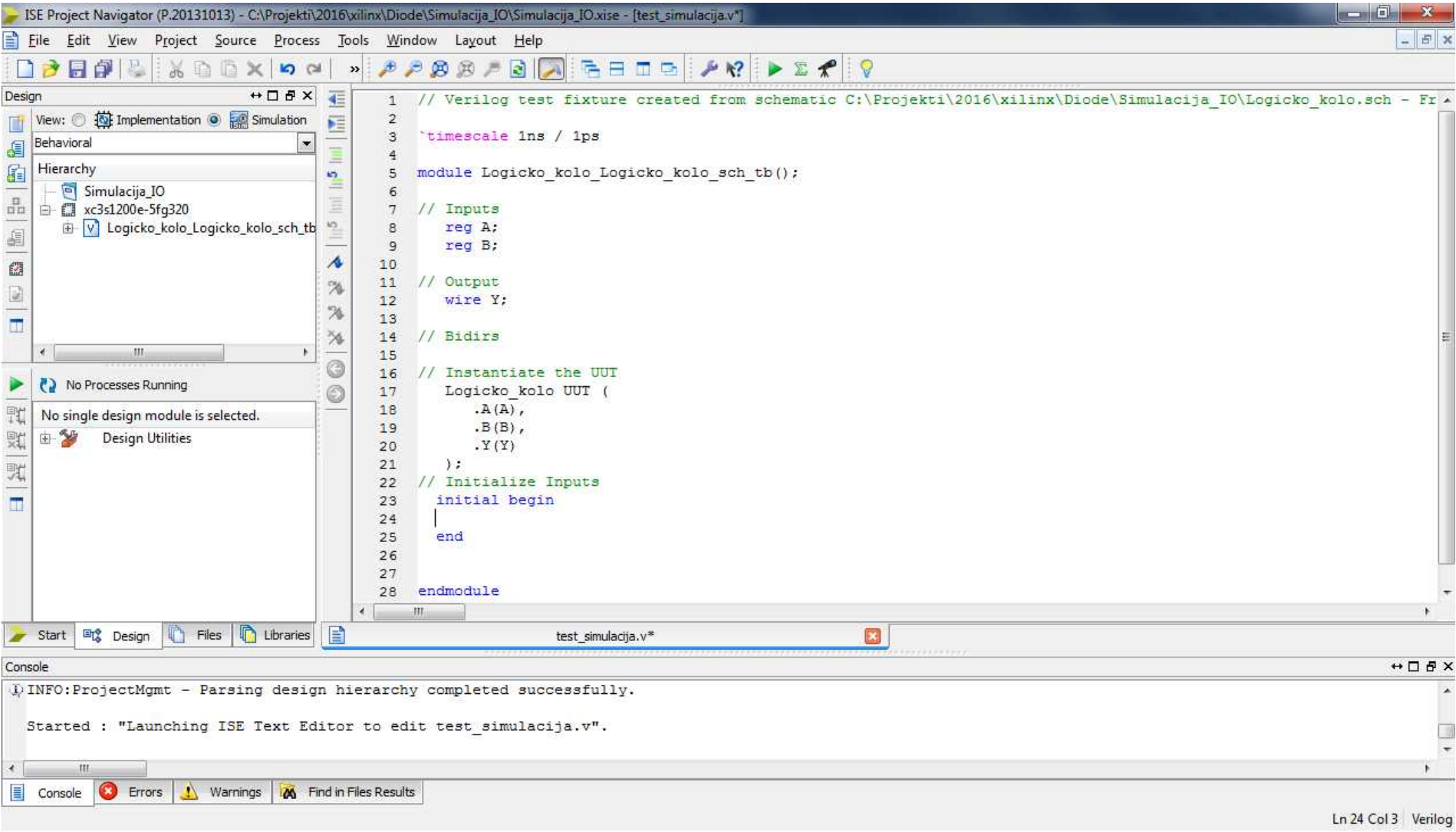
Otvara se fajl u kome definisemo ulaze

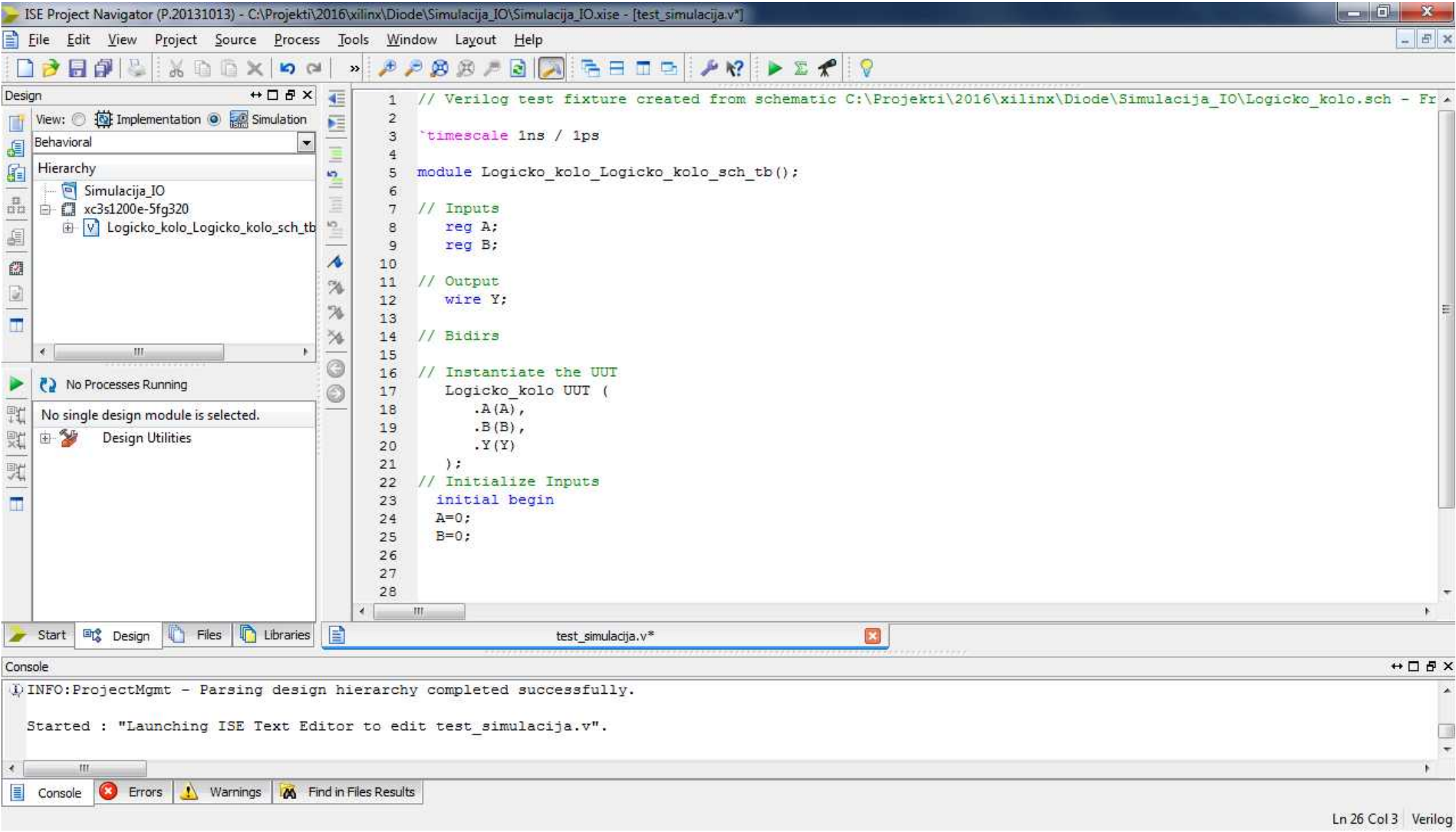


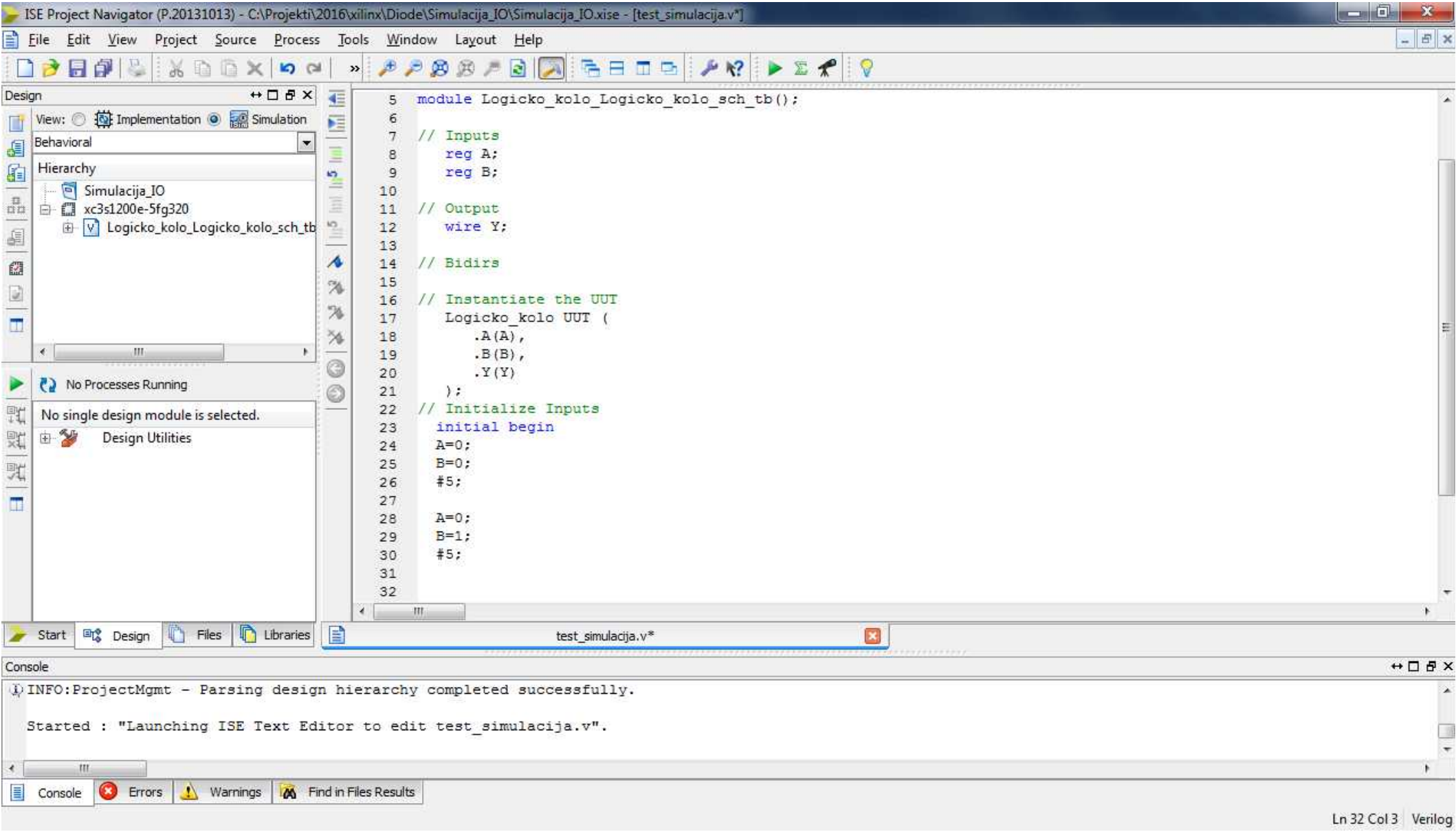
Selektujemo I obrisemo definisano stanje

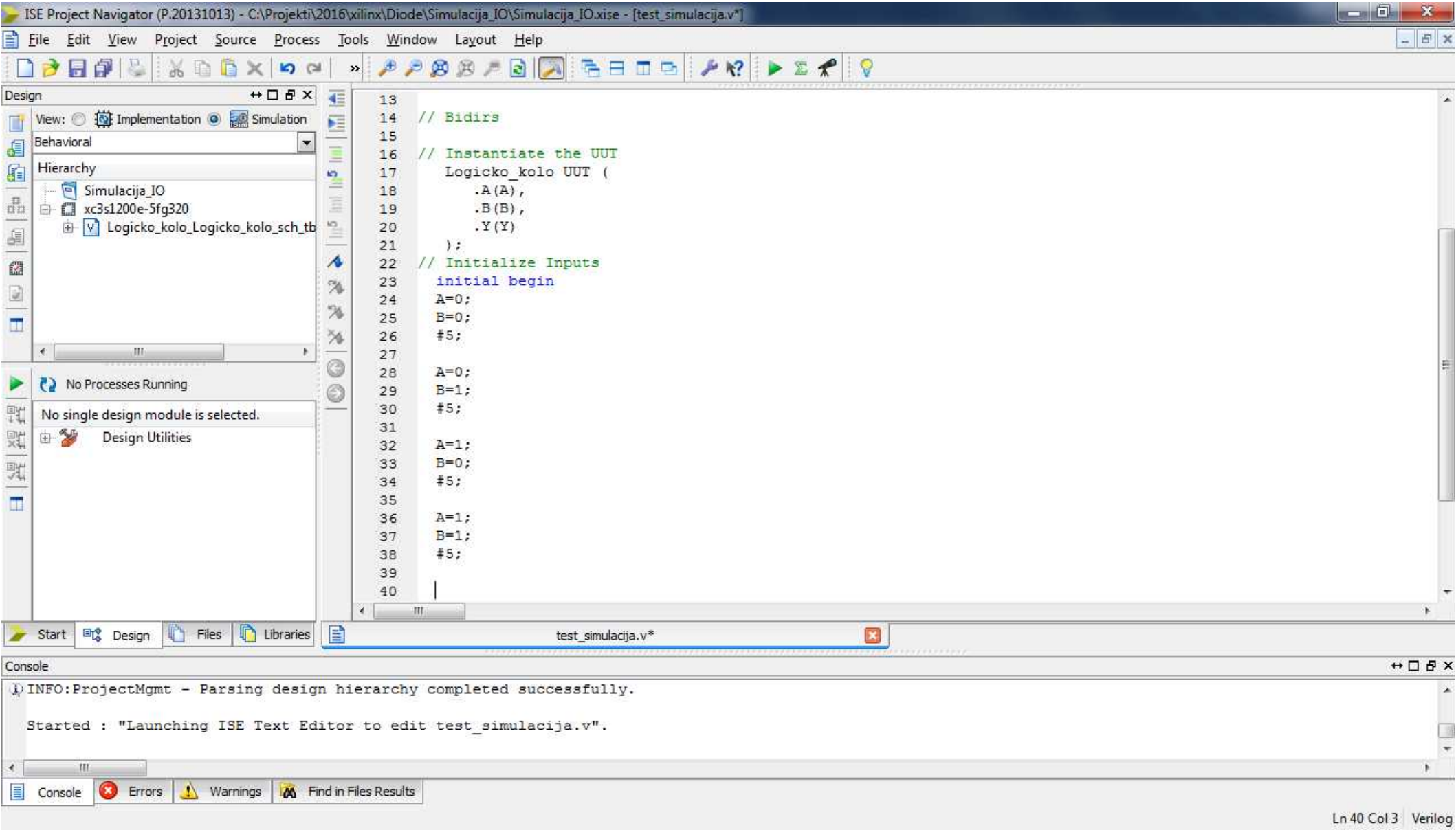


Unutar initial begin I end definisemo ulaze

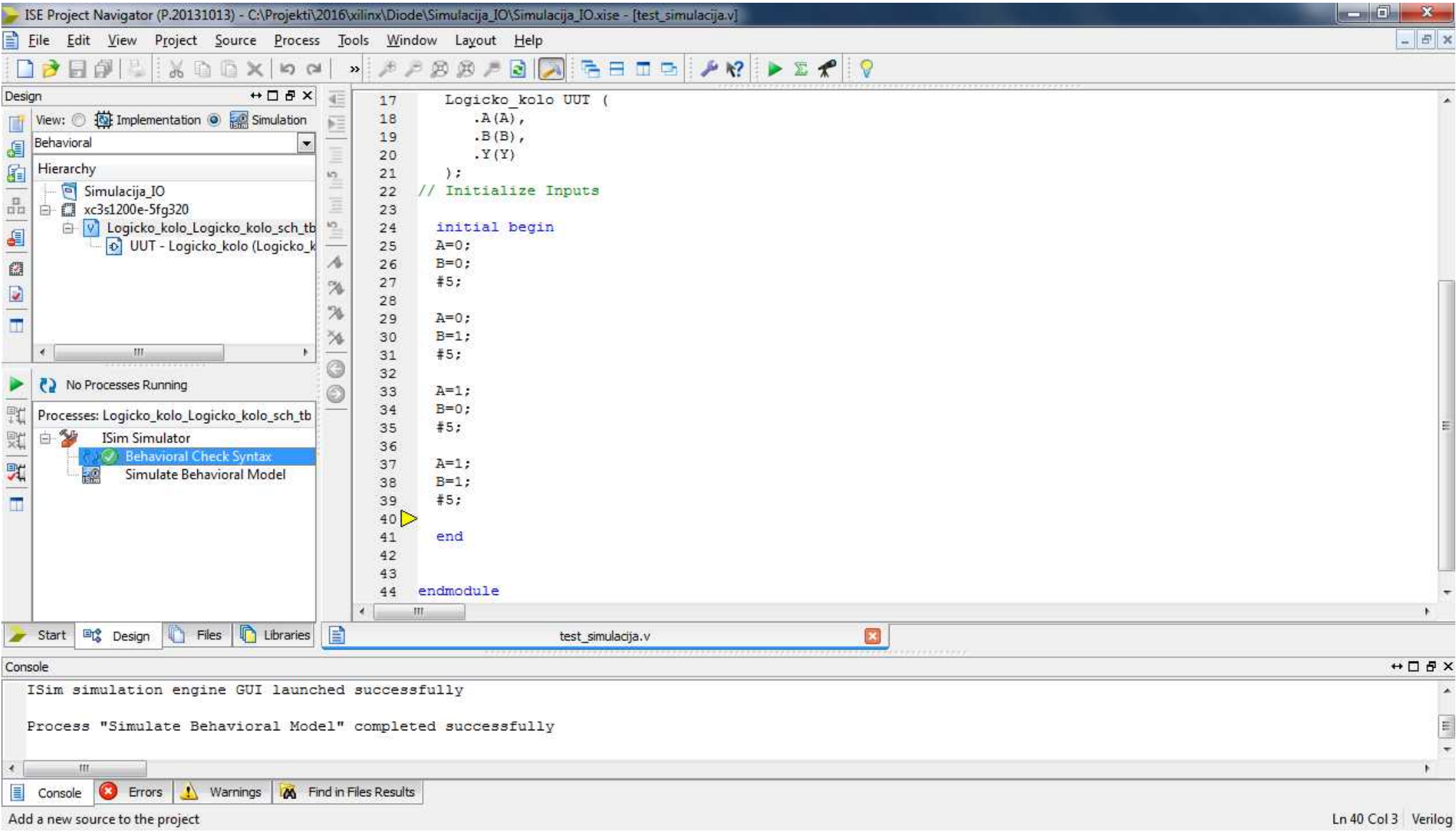



ISE Project Navigator (P.20131013) - C:\Projekti\2016\xilinx\Diode\Simulacija_IO\Simulacija_IO.xise - [test_simulacija.v*]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
Simulacija_IO
xc3s1200e-5fg320
Logicko_kolo_Logicko_kolo_sch_tb
No Processes Running
No single design module is selected.
Design Utilities
Start Design Files Libraries
1 // Verilog test fixture created from schematic C:\Projekti\2016\xilinx\Diode\Simulacija_IO\Logicko_kolo.sch - Fr
2
3 `timescale 1ns / 1ps
4
5 module Logicko_kolo_Logicko_kolo_sch_tb();
6
7 // Inputs
8 reg A;
9 reg B;
10
11 // Output
12 wire Y;
13
14 // Bidirs
15
16 // Instantiate the UUT
17 Logicko_kolo UUT (
18 .A(A),
19 .B(B),
20 .Y(Y)
21);
22 // Initialize Inputs
23 initial begin
24 A=0;
25 B=0;
26
27
28
test_simulacija.v*
Console
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.
Started : "Launching ISE Text Editor to edit test_simulacija.v".
Console Errors Warnings Find in Files Results
Ln 26 Col 3 Verilog

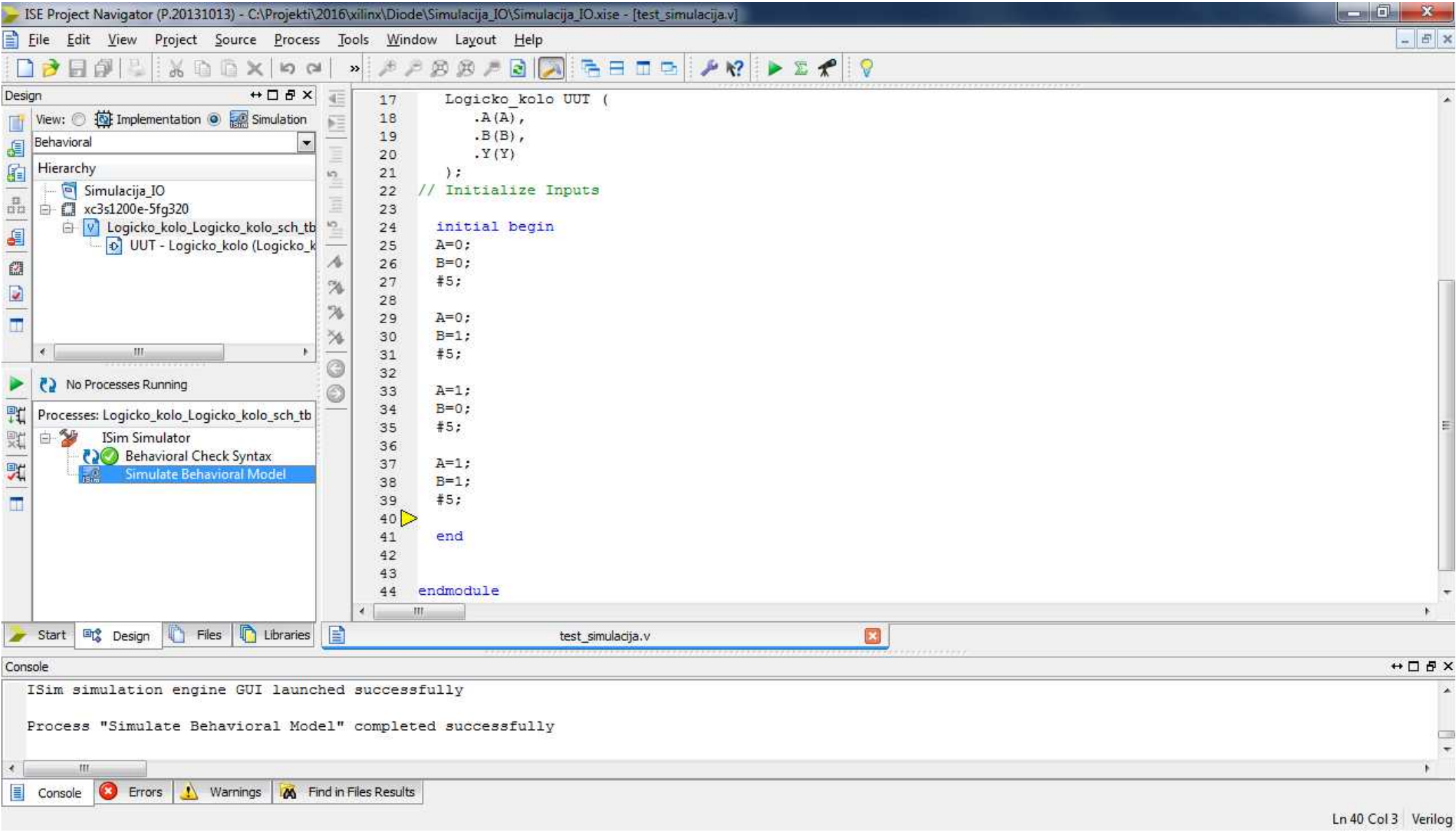

ISE Project Navigator (P.20131013) - C:\Projekti\2016\xilinx\Diode\Simulacija_IO\Simulacija_IO.xise - [test_simulacija.v*]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
Simulacija_IO
xc3s1200e-5fg320
Logicko_kolo_Logicko_kolo_sch_tb
No Processes Running
No single design module is selected.
Design Utilities
Start Design Files Libraries
5 module Logicko_kolo_Logicko_kolo_sch_tb();
6
7 // Inputs
8 reg A;
9 reg B;
10
11 // Output
12 wire Y;
13
14 // Bidirs
15
16 // Instantiate the UUT
17 Logicko_kolo UUT (
18 .A(A),
19 .B(B),
20 .Y(Y)
21);
22 // Initialize Inputs
23 initial begin
24 A=0;
25 B=0;
26 #5;
27
28 A=0;
29 B=1;
30 #5;
31
32
test_simulacija.v*
Console
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.
Started : "Launching ISE Text Editor to edit test_simulacija.v".
Console Errors Warnings Find in Files Results
Ln 32 Col 3 Verilog

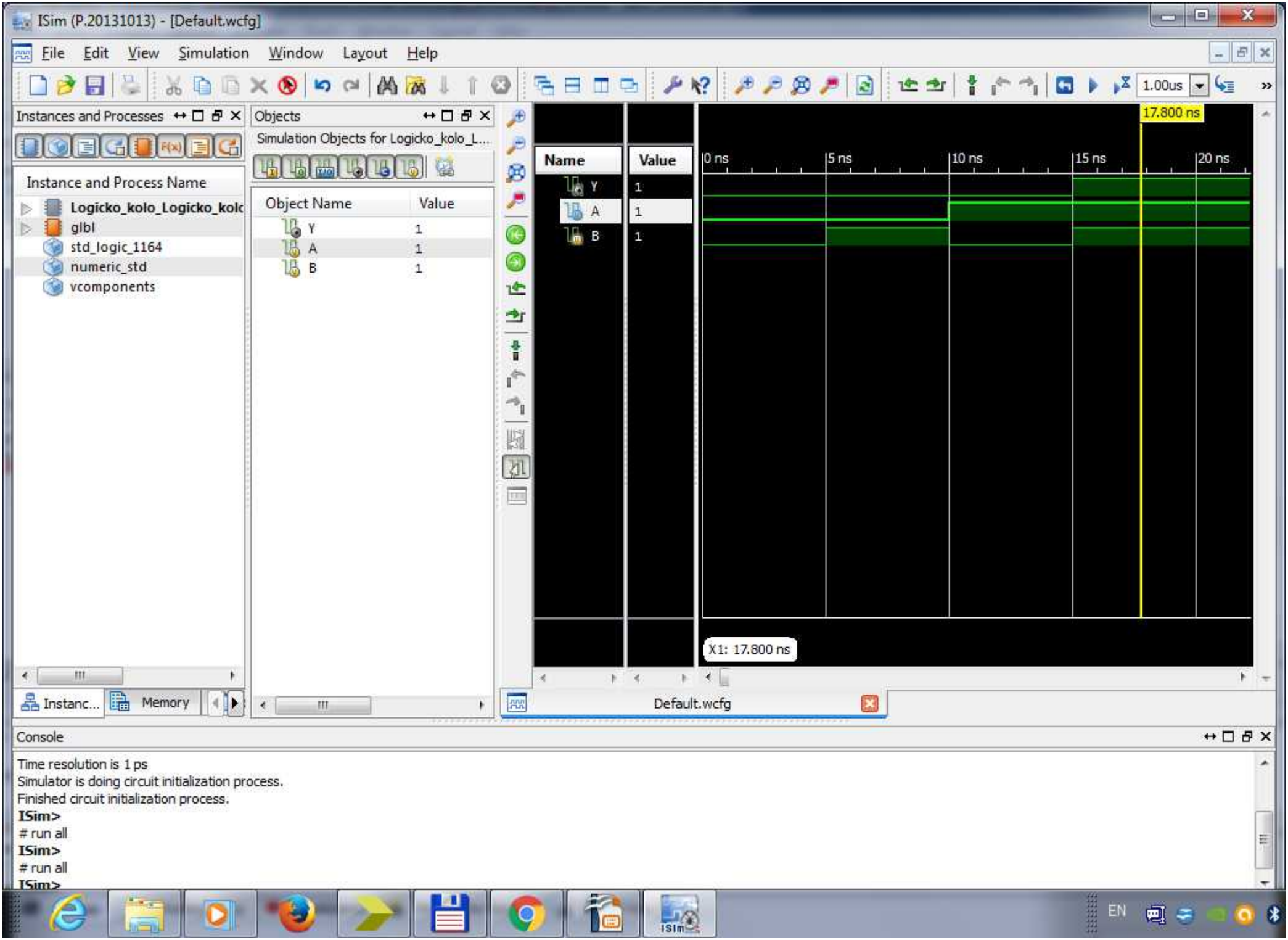

ISE Project Navigator (P.20131013) - C:\Projekti\2016\xilinx\Diode\Simulacija_IO\Simulacija_IO.xise - [test_simulacija.v*]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
Simulacija_IO
xc3s1200e-5fg320
Logicko_kolo_Logicko_kolo_sch_tb
No Processes Running
No single design module is selected.
Design Utilities
Start Design Files Libraries
13
14 // Bidirs
15
16 // Instantiate the UUT
17 Logicko_kolo UUT (
18 .A(A),
19 .B(B),
20 .Y(Y)
21);
22 // Initialize Inputs
23 initial begin
24 A=0;
25 B=0;
26 #5;
27
28 A=0;
29 B=1;
30 #5;
31
32 A=1;
33 B=0;
34 #5;
35
36 A=1;
37 B=1;
38 #5;
39
40
test_simulacija.v*
Console
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.
Started : "Launching ISE Text Editor to edit test_simulacija.v".
Console Errors Warnings Find in Files Results
Ln 40 Col 3 Verilog

Dupli Klik na Behavioral Check Syntax

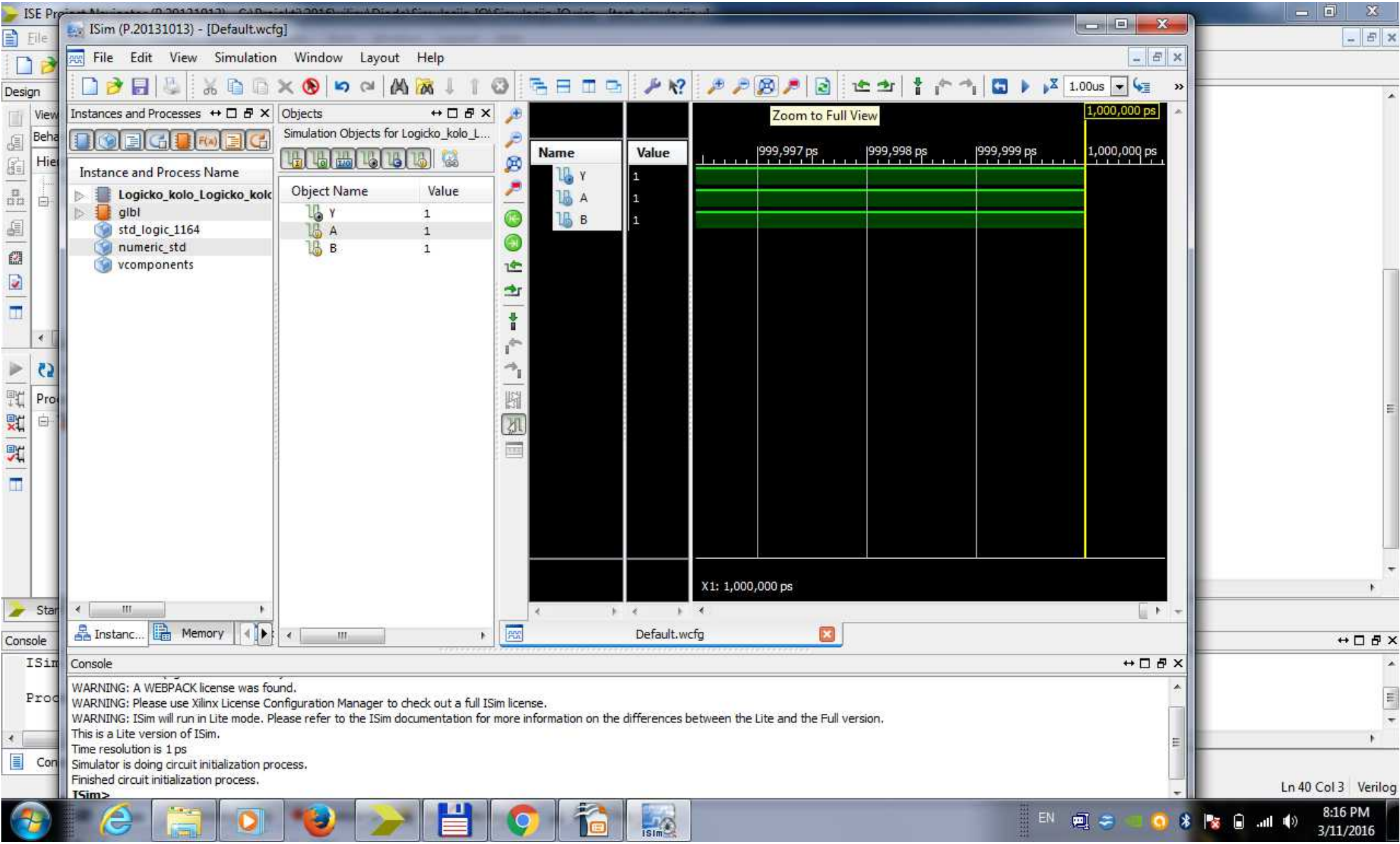


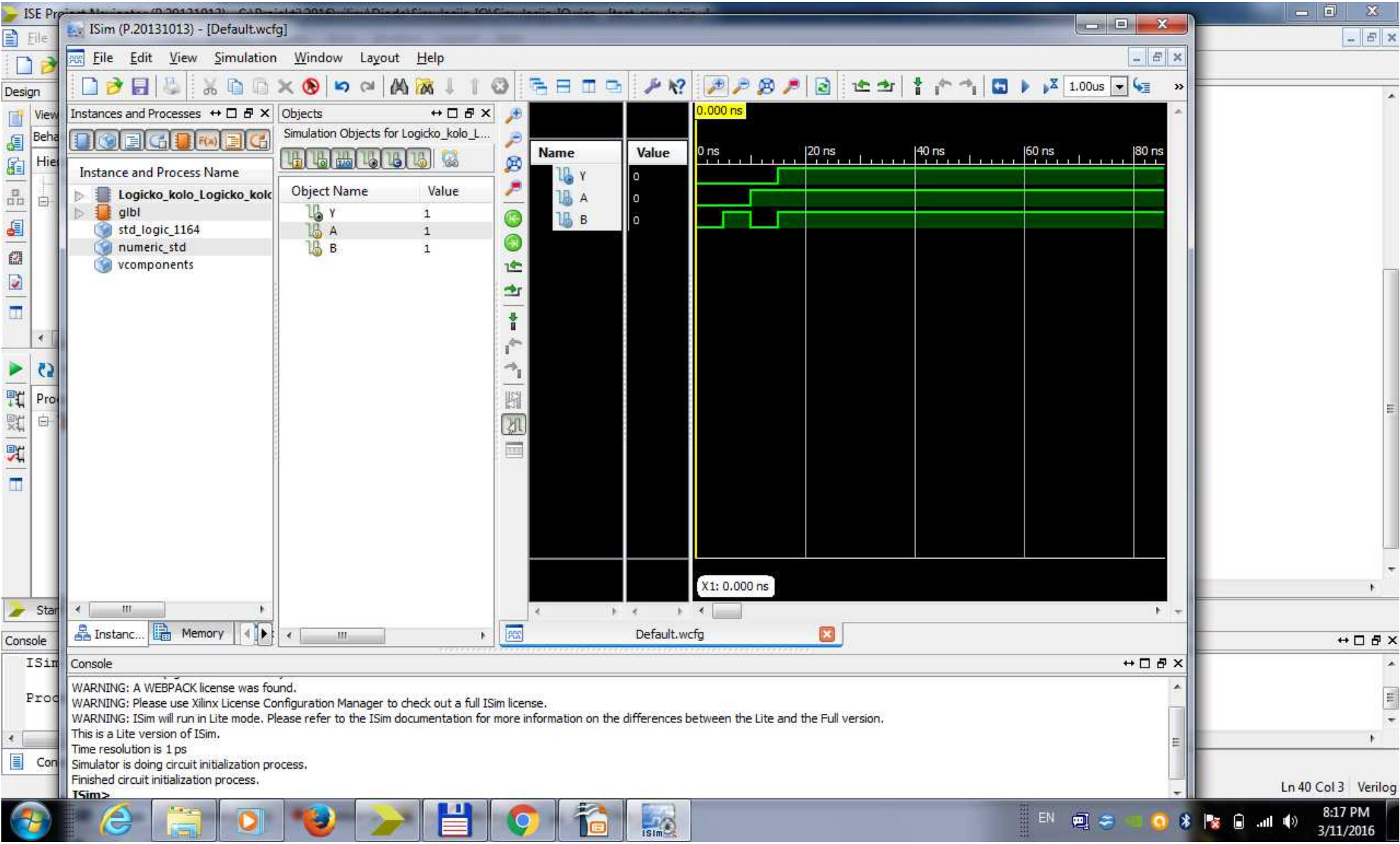
Svako stanje definisali smo da traje 5 ciklusa, 5ns, #5
Dupli klik na Simulate Behavioral Model I pokrecemo ISim

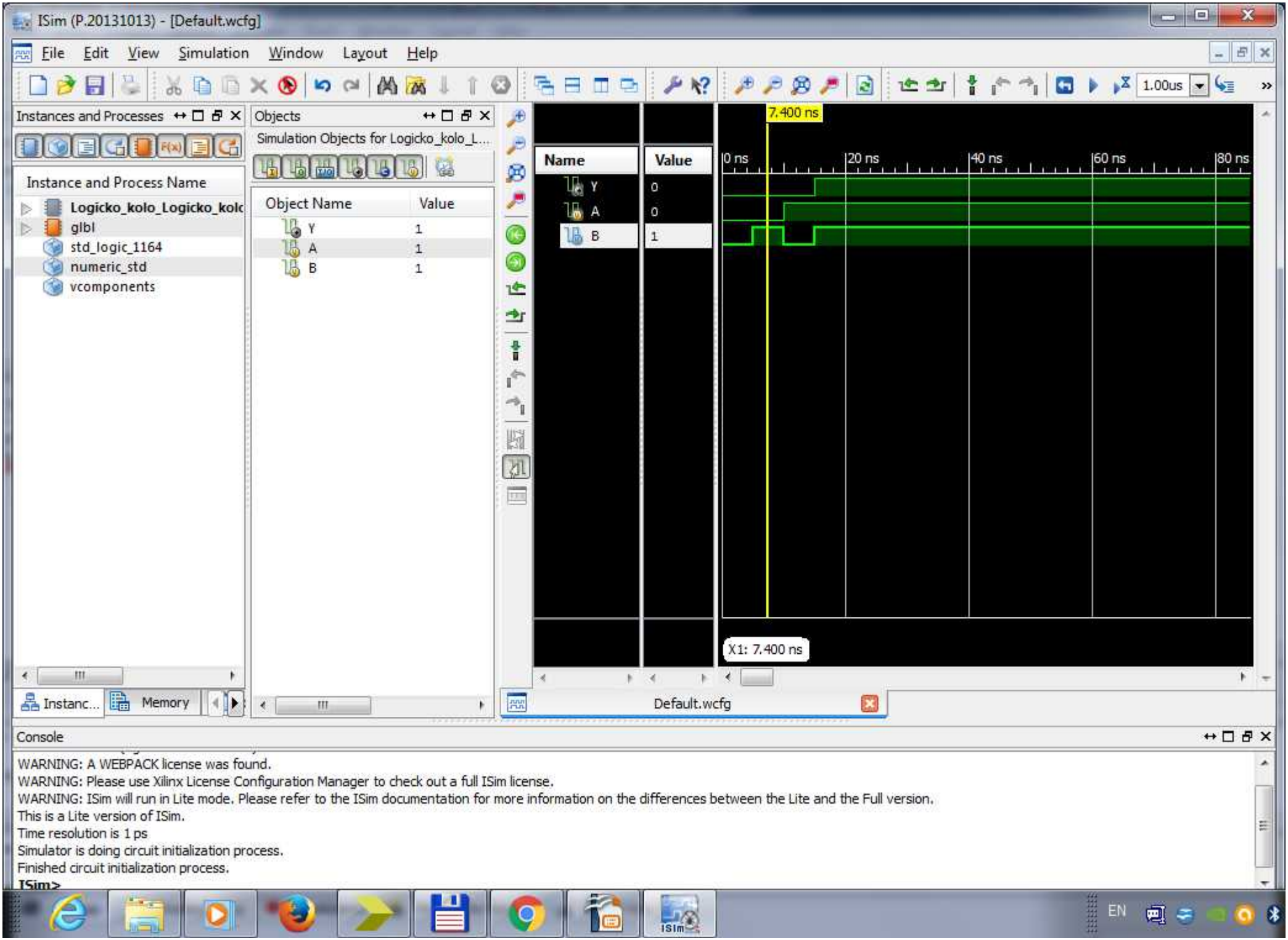



ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Instances and Processes
Instance and Process Name
Logicko_kolo_Logicko_kolc
glbl
std_logic_1164
numeric_std
vcomponents
Objects
Simulation Objects for Logicko_kolo_L...
Object Name Value
Y 1
A 1
B 1
Name Value
Y 1
A 1
B 1
0 ns 5 ns 10 ns 15 ns 20 ns
17.800 ns
X1: 17.800 ns
Default.wcfg
Console
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>
run all
ISim>
run all
ISim>

Na zoom zumiramo ulazne signale I pomeranjem klizaca pratimo stanja




ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Instances and Processes
Instance and Process Name
Logicko_kolo_Logicko_kolc
glbl
std_logic_1164
numeric_std
vcomponents
Objects
Simulation Objects for Logicko_kolo_L...
Object Name
Value
Y 1
A 1
B 1
Name
Value
Y 0
A 0
B 0
0.000 ns
0 ns
20 ns
40 ns
60 ns
80 ns
X1: 0.000 ns
1.00us
Instanc...
Memory
Default.wcfg
Console
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>


ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Instances and Processes
Instance and Process Name
Logicko_kolo_Logicko_kolc
glbl
std_logic_1164
numeric_std
vcomponents
Instanc...
Memory
Objects
Simulation Objects for Logicko_kolo_L...
Object Name
Value
Y 1
A 1
B 1
Name
Value
Y 0
A 0
B 1
7.400 ns
0 ns
20 ns
40 ns
60 ns
80 ns
X1: 7.400 ns
Default.wcfg
Console
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>