

Simulacija rada logickog kola

Otvorimo novi projekata, izaberemo Schematik

ISE Project Navigator (P.20131013) - C:\Projekti\2016\wilinx\Diode\Simulacija_IO\Simulacija_IO.xise - [Logicko_kolo.sch]

File Edit View Project Source Process Add Tools Window Layout Help

Options

Select Options

When you click on a branch:

- Select the entire branch
- Select the line segment

When you move an object:

- Keep the connections to other objects
- Break the connections to other objects

When you use the area select tool, select the objects that:

- Are enclosed by the area
- Intersect the area

When you use the area select tool, select:

- Objects including attribute windows
- Objects excluding attribute windows

Libraries Symbols Options Logicko_kolo.sch

Console

```
Process "Creating Schematic" completed successfully  
Started : "Launching Schematic Editor to edit Logicko_kolo.sch".
```

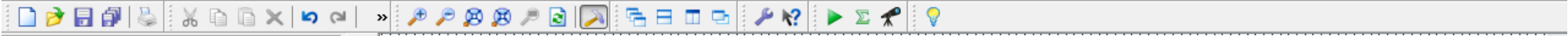
Console Errors Warnings Find in Files Results

Izaberemo simulaciju jednostavnog AND kola

The screenshot displays the ISE Project Navigator interface. The main window is the Schematic Editor, showing a single AND gate symbol on a blank canvas. The left sidebar contains the 'Options' panel, which is currently expanded to show 'Select Options'. The console window at the bottom shows the following text:

```
Process "Creating Schematic" completed successfully  
Started : "Launching Schematic Editor to edit Logicko_kolo.sch".
```

The status bar at the bottom right indicates the coordinates [1060,1420].



Options

Select Options

When you click on a branch:

- Select the entire branch
- Select the line segment

When you move an object:

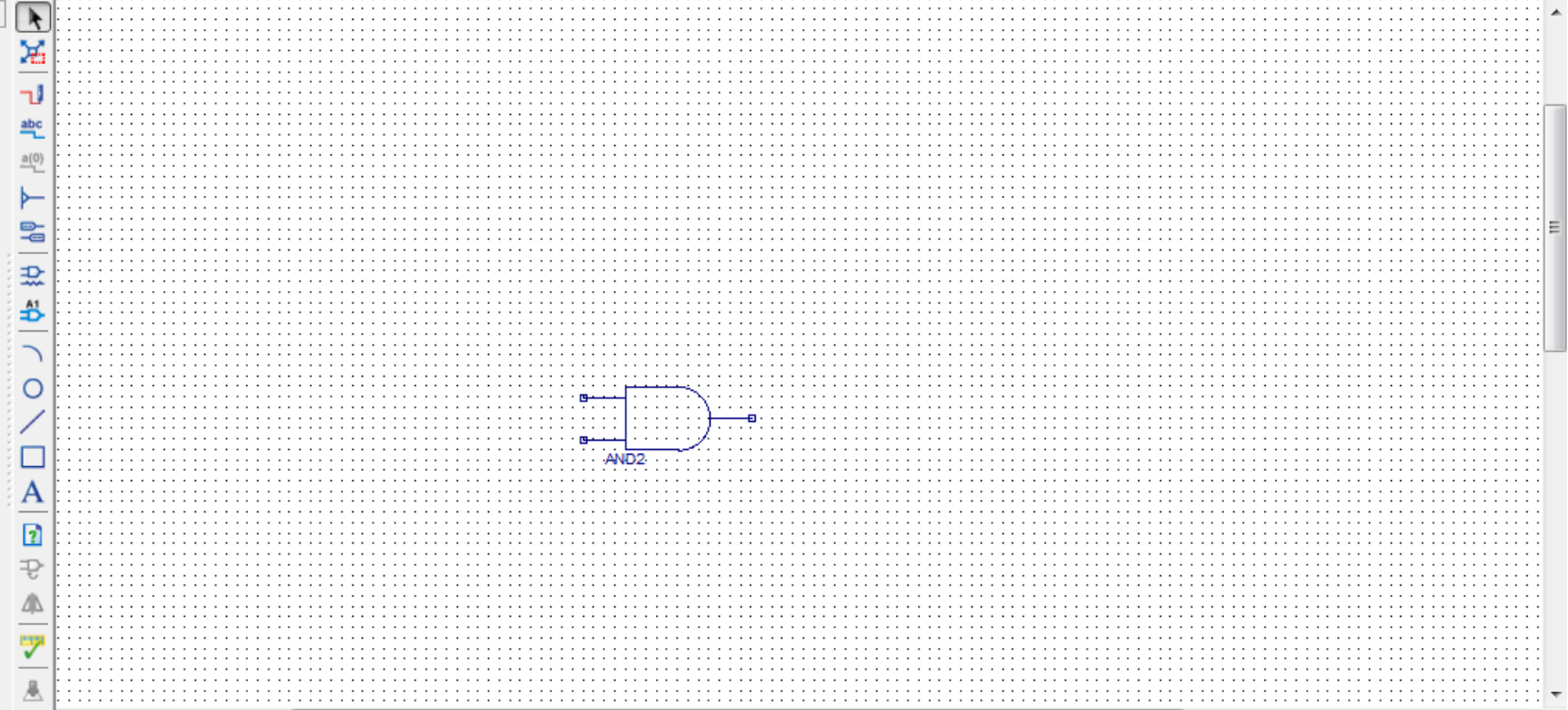
- Keep the connections to other objects
- Break the connections to other objects

When you use the area select tool, select the objects that:

- Are enclosed by the area
- Intersect the area

When you use the area select tool, select:

- Objects including attribute windows
- Objects excluding attribute windows



```
Process "Creating Schematic" completed successfully  
  
Started : "Launching Schematic Editor to edit Logicko_kolo.sch".
```

Dodamo ulaze I izlaz

The screenshot displays the ISE Project Navigator interface. The main window is the Schematic Editor, showing a grid with a single AND gate component labeled "AND2". The left input of the AND gate is connected to a signal source labeled "XLXN_1". The right input of the AND gate is unconnected. The output of the AND gate is also unconnected. The interface includes a menu bar (File, Edit, View, Project, Source, Process, Add, Tools, Window, Layout, Help), a toolbar with various icons, and an "Options" panel on the left. The "Options" panel has four sections: "When you click on a branch:", "When you move an object:", "When you use the area select tool, select the objects that:", and "When you use the area select tool, select:". The "Console" window at the bottom shows the following text:

```
Process "Creating Schematic" completed successfully  
  
Started : "Launching Schematic Editor to edit Logicko_kolo.sch".
```

The status bar at the bottom of the console window shows "Console", "Errors", "Warnings", and "Find in Files Results".



Options

Select Options

When you click on a branch:

- Select the entire branch
- Select the line segment

When you move an object:

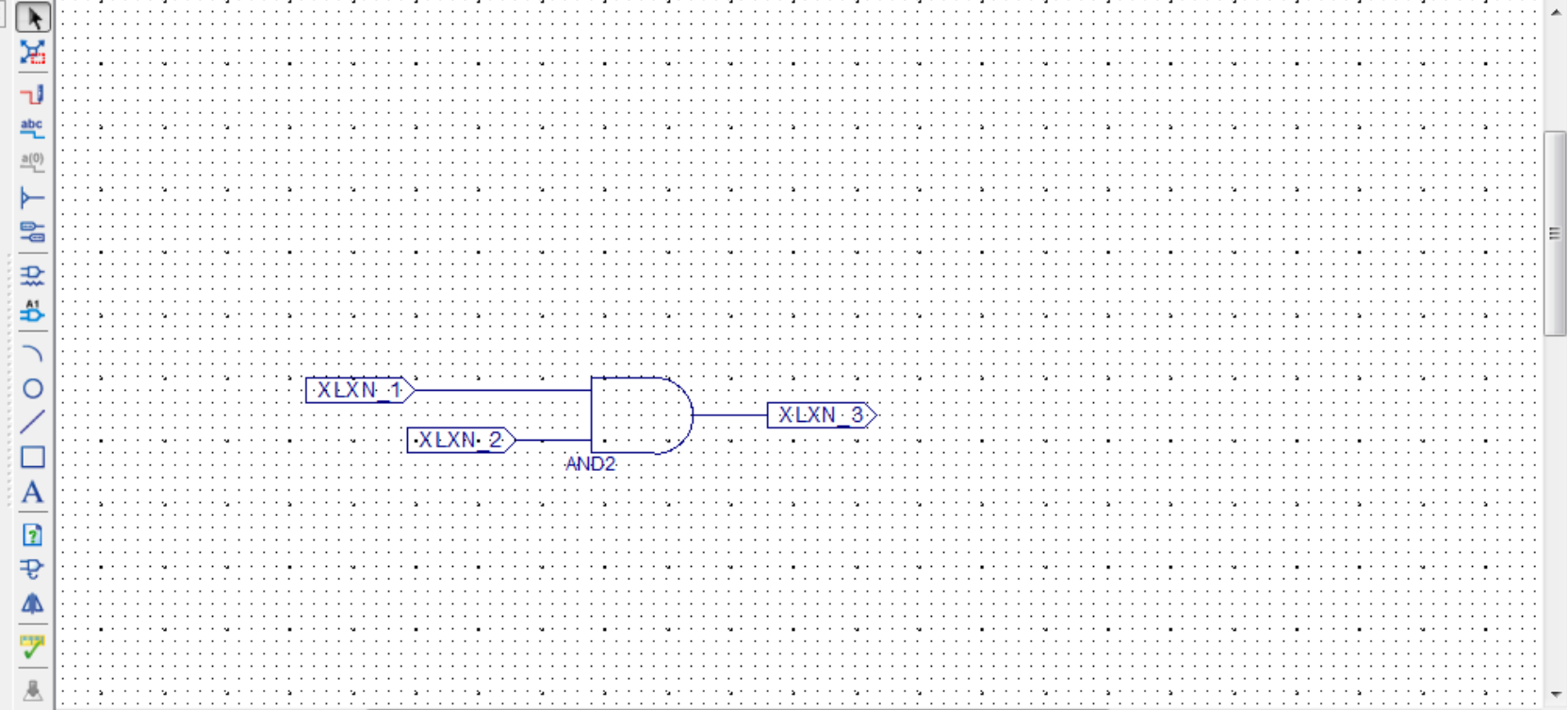
- Keep the connections to other objects
- Break the connections to other objects

When you use the area select tool, select the objects that:

- Are enclosed by the area
- Intersect the area

When you use the area select tool, select:

- Objects including attribute windows
- Objects excluding attribute windows



```
Process "Creating Schematic" completed successfully  
  
Started : "Launching Schematic Editor to edit Logicko_kolo.sch".
```



Options

Select Options

When you click on a branch:

- Select the entire branch
- Select the line segment

When you move an object:

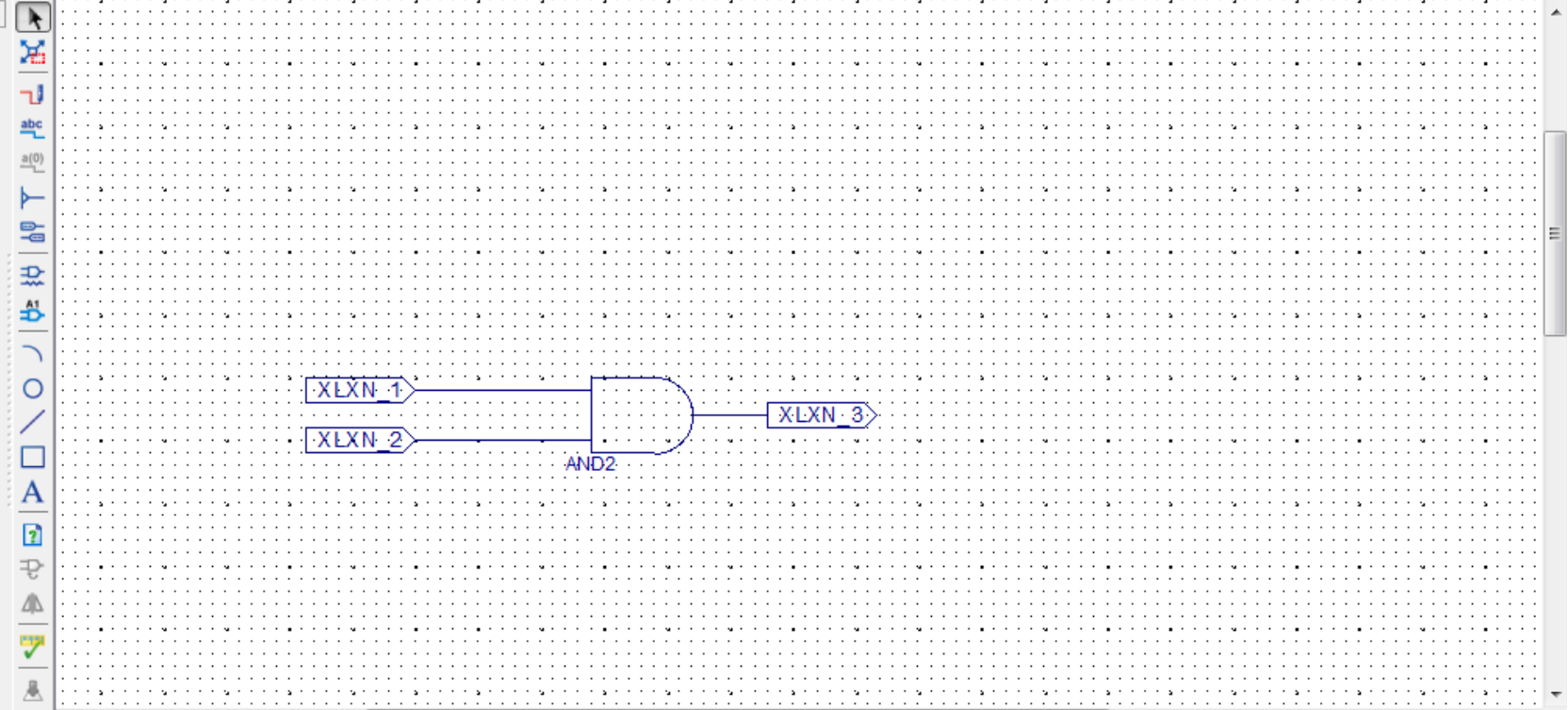
- Keep the connections to other objects
- Break the connections to other objects

When you use the area select tool, select the objects that:

- Are enclosed by the area
- Intersect the area

When you use the area select tool, select:

- Objects including attribute windows
- Objects excluding attribute windows



```
Process "Creating Schematic" completed successfully  
  
Started : "Launching Schematic Editor to edit Logicko_kolo.sch".
```

Desni klik na IO, izaberemo Rename I ulazima dodelimo ime A I B, a izlazu Y

The screenshot displays the ISE Project Navigator interface. The main workspace is a schematic editor with a grid background. A context menu is open over an IO pin labeled "X:LN 3". The menu items are:

- Cut (Ctrl+X)
- Copy (Ctrl+C)
- Paste (Ctrl+V)
- Paste Special...
- Delete (Del)
- Zoom
- Select and Clear
- Mirror
- Rotate
- Rename Port** (highlighted)
- Object Properties (Alt+Enter)
- Preferences...

The left sidebar contains the "Options" panel with the following settings:

- When you click on a branch:
 - Select the entire branch
 - Select the line segment
- When you move an object:
 - Keep the connections to other objects
 - Break the connections to other objects
- When you use the area select tool, select the objects that:
 - Are enclosed by the area
 - Intersect the area
- When you use the area select tool, select:
 - Objects including attribute windows
 - Objects excluding attribute windows

The console window at the bottom shows the following messages:

```
Process "Creating Schematic" completed successfully
Started : "Launching Schematic Editor to edit Logicko_kolo.sch".
```

The system tray at the bottom right shows the date and time: 7:50 PM, 3/11/2016.



Options

Select Options

When you click on a branch:

- Select the entire branch
- Select the line segment

When you move an object:

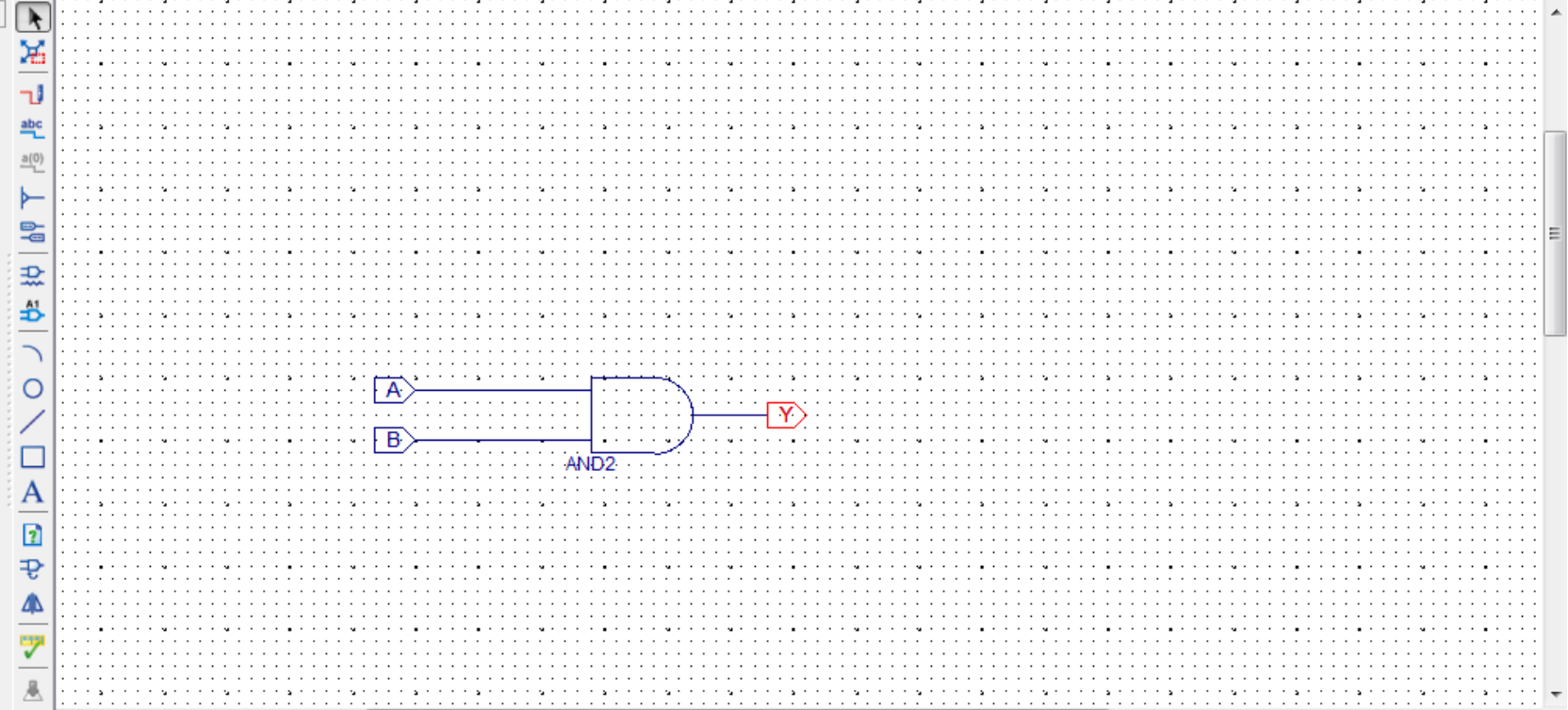
- Keep the connections to other objects
- Break the connections to other objects

When you use the area select tool, select the objects that:

- Are enclosed by the area
- Intersect the area

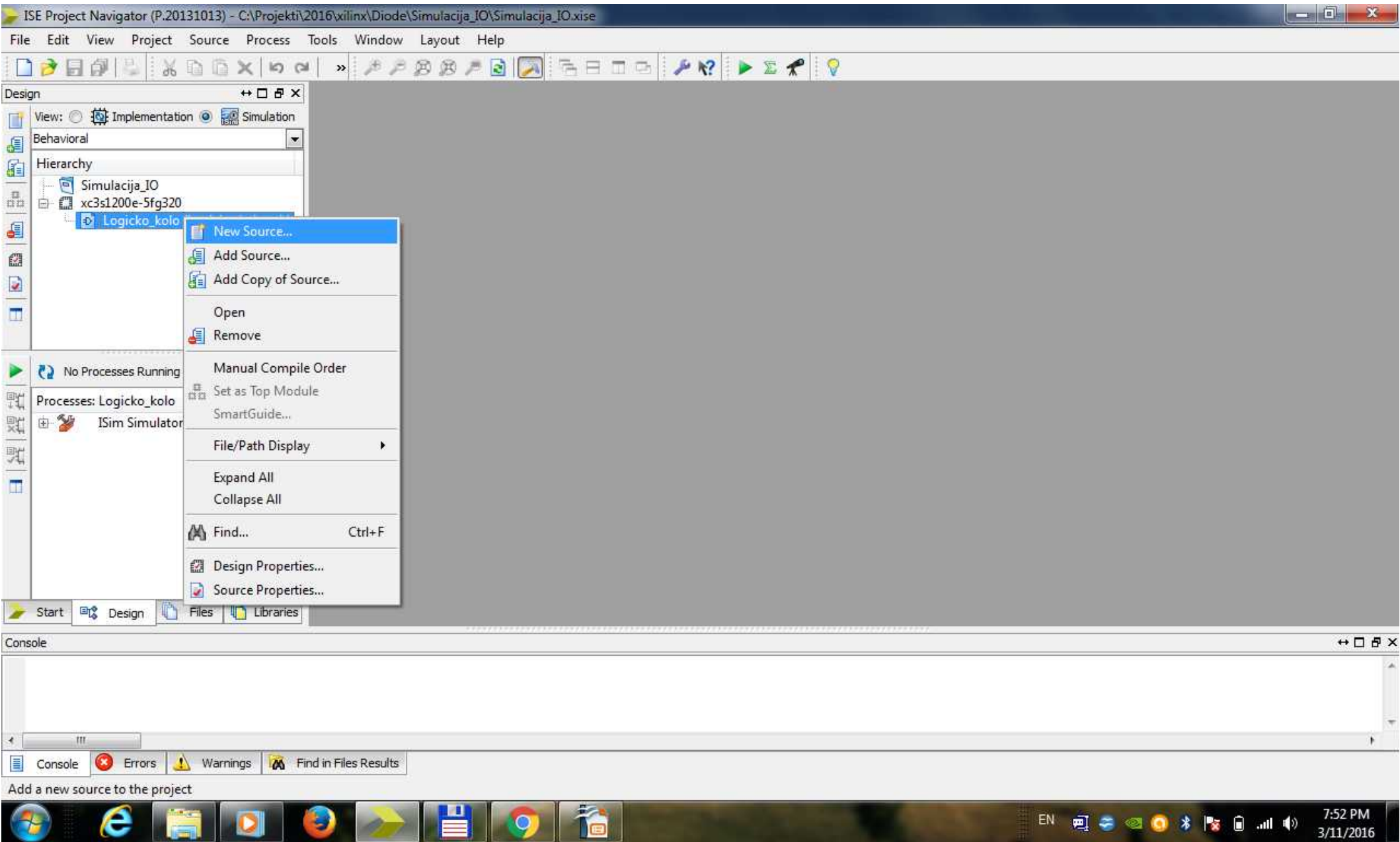
When you use the area select tool, select:

- Objects including attribute windows
- Objects excluding attribute windows

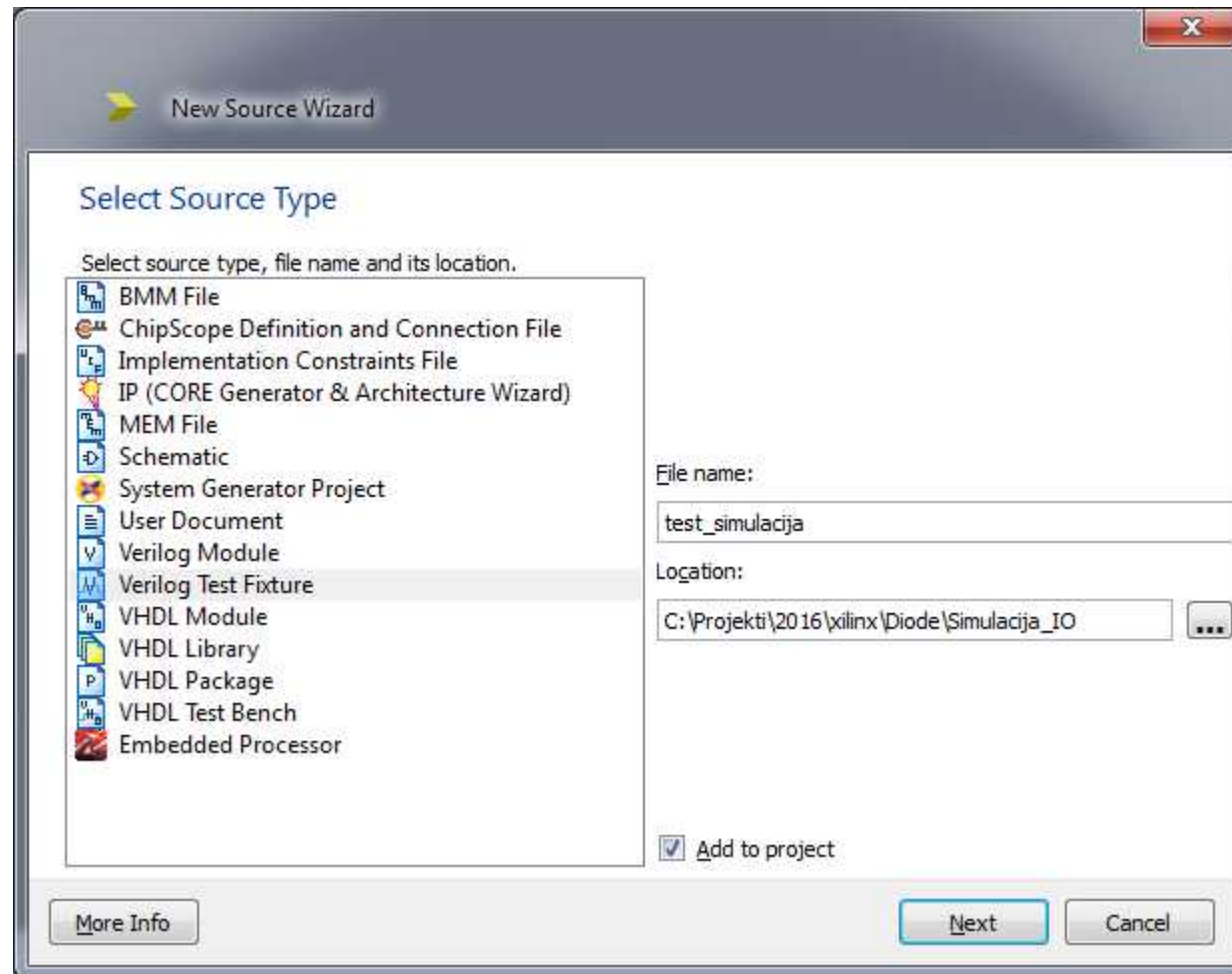


```
Process "Creating Schematic" completed successfully  
  
Started : "Launching Schematic Editor to edit Logicko_kolo.sch".
```

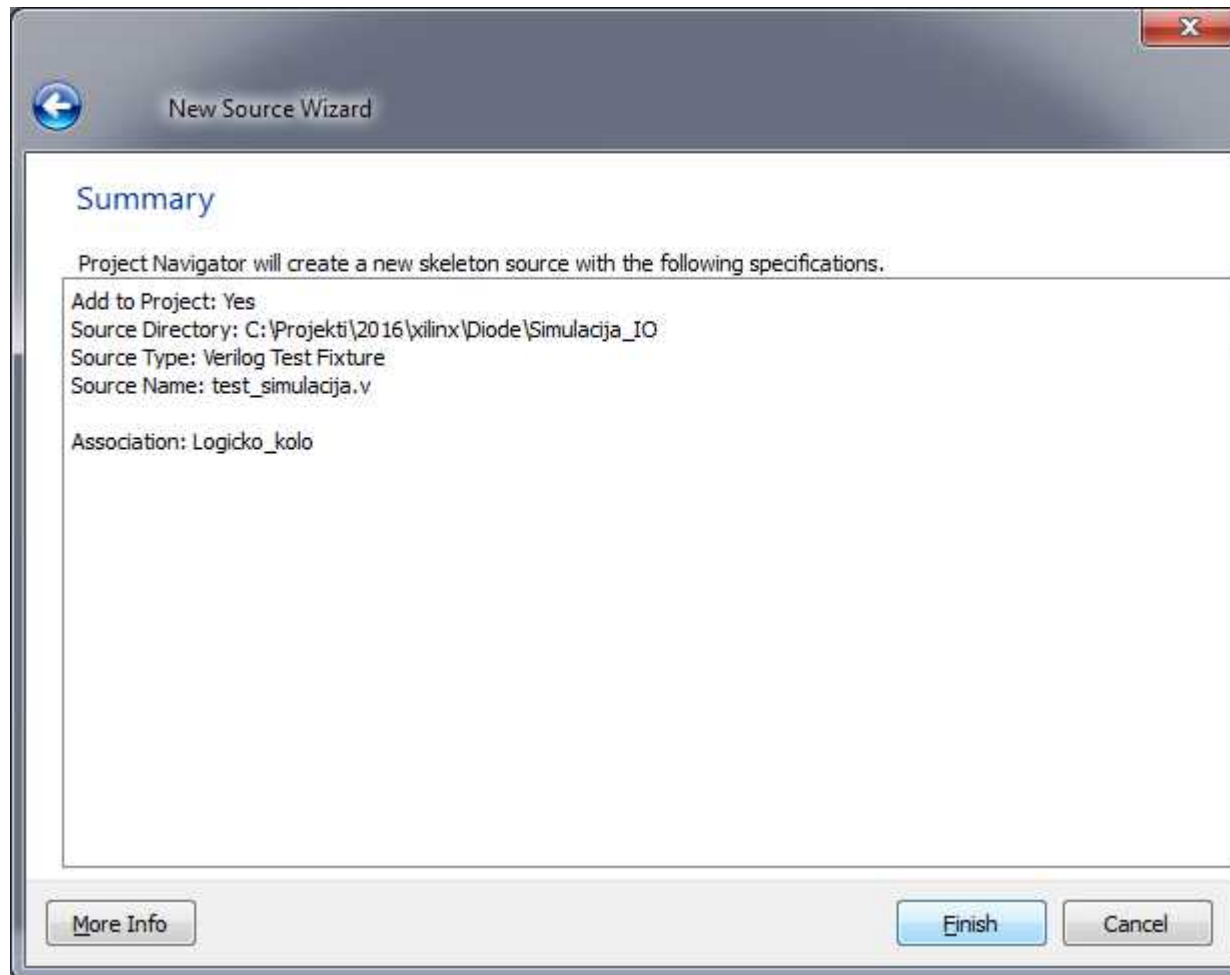
Klik na logicko kolo, pa New Source...



Selektujemo Verilog Test Fixture, dodamo ime na primer test_simulacija



Klik na Finish



Otvora se fajl u kome definisemo ulaze

The screenshot displays the ISE Project Navigator interface. The main window shows a Verilog test fixture file named `test_simulacija.v` with the following code:

```
1 // Verilog test fixture created from schematic C:\Projekti\2016\xilinx\Diode\Simulacija_IO\Logicko_kolo.sch - Fr
2
3 `timescale 1ns / 1ps
4
5 module Logicko_kolo_Logicko_kolo_sch_tb();
6
7 // Inputs
8   reg A;
9   reg B;
10
11 // Output
12   wire Y;
13
14 // Bidirs
15
16 // Instantiate the UUT
17   Logicko_kolo UUT (
18     .A(A),
19     .B(B),
20     .Y(Y)
21   );
22 // Initialize Inputs
23 `ifdef auto_init
24   initial begin
25     A = 0;
26     B = 0;
27   `endif
28 endmodule
```

The left sidebar shows the Design view with the Hierarchy tree expanded to `Logicko_kolo_Logicko_kolo_sch_tb`. The Console window at the bottom shows the following output:

```
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.
Started : "Launching ISE Text Editor to edit test_simulacija.v".
```

The status bar at the bottom right indicates the current position is `Ln 1 Col 1` in a `Verilog` file.

Selektujemo I obrisemo definisano stanje

The screenshot displays the ISE Project Navigator interface. The main window shows the Verilog source code for a testbench named `Logicko_kolo_Logicko_kolo_sch_tb()`. The code includes a timescale, module definition, input and output declarations, and an initial state block. The initial state block is highlighted in grey, showing the initialization of variables A and B to 0.

```
2
3 `timescale 1ns / 1ps
4
5 module Logicko_kolo_Logicko_kolo_sch_tb();
6
7 // Inputs
8   reg A;
9   reg B;
10
11 // Output
12   wire Y;
13
14 // Bidirs
15
16 // Instantiate the UUT
17   Logicko_kolo UUT (
18     .A(A),
19     .B(B),
20     .Y(Y)
21   );
22 // Initialize Inputs
23 `ifdef auto_init
24     initial begin
25         A = 0;
26         B = 0;
27     `endif
28 endmodule
29
```

The left sidebar shows the Design view with the Hierarchy tree expanded to the selected module `Logicko_kolo_Logicko_kolo_sch_tb`. The bottom status bar indicates the current file is `test_simulacija.v` at line 23, column 3.

Console output:

```
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.
Started : "Launching ISE Text Editor to edit test_simulacija.v".
```

Unutar initial begin I end definisemo ulaze

The screenshot displays the Xilinx ISE Project Navigator interface. The main window shows a Verilog test fixture for a logic circuit. The code defines a module named `Logicko_kolo_Logicko_kolo_sch_tb()` with two input registers (`A` and `B`), one output wire (`Y`), and an instantiation of the circuit under test (`Logicko_kolo UUT`). The test fixture includes an `initial` block to initialize the inputs.

```
1 // Verilog test fixture created from schematic C:\Projekti\2016\xilinx\Diode\Simulacija_IO\Logicko_kolo.sch - Fr
2
3 `timescale 1ns / 1ps
4
5 module Logicko_kolo_Logicko_kolo_sch_tb();
6
7 // Inputs
8   reg A;
9   reg B;
10
11 // Output
12   wire Y;
13
14 // Bidirs
15
16 // Instantiate the UUT
17   Logicko_kolo UUT (
18     .A(A),
19     .B(B),
20     .Y(Y)
21   );
22 // Initialize Inputs
23   initial begin
24     |
25   end
26
27
28 endmodule
```

The console window at the bottom shows the following output:

```
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.
Started : "Launching ISE Text Editor to edit test_simulacija.v".
```

The status bar at the bottom right indicates the current position in the code: `Ln 24 Col 3 Verilog`.



Design

View: Implementation Simulation

Behavioral

Hierarchy

- Simulacija_IO
 - xc3s1200e-5fg320
 - Logicko_kolo_Logicko_kolo_sch_tb

No Processes Running

No single design module is selected.

Design Utilities

```
1 // Verilog test fixture created from schematic C:\Projekti\2016\xilinx\Diode\Simulacija_IO\Logicko_kolo.sch - Fr
2
3 `timescale 1ns / 1ps
4
5 module Logicko_kolo_Logicko_kolo_sch_tb();
6
7 // Inputs
8   reg A;
9   reg B;
10
11 // Output
12   wire Y;
13
14 // Bidirs
15
16 // Instantiate the UUT
17   Logicko_kolo UUT (
18     .A(A),
19     .B(B),
20     .Y(Y)
21   );
22 // Initialize Inputs
23   initial begin
24     A=0;
25     B=0;
26
27
28
```

INFO:ProjectMgmt - Parsing design hierarchy completed successfully.

Started : "Launching ISE Text Editor to edit test_simulacija.v".



Design

View: Implementation Simulation

Behavioral

Hierarchy

- Simulacija_IO
 - xc3s1200e-5fg320
 - Logicko_kolo_Logicko_kolo_sch_tb

No Processes Running

No single design module is selected.

Design Utilities

```
5 module Logicko_kolo_Logicko_kolo_sch_tb();
6
7 // Inputs
8 reg A;
9 reg B;
10
11 // Output
12 wire Y;
13
14 // Bidirs
15
16 // Instantiate the UUT
17 Logicko_kolo UUT (
18     .A(A),
19     .B(B),
20     .Y(Y)
21 );
22 // Initialize Inputs
23 initial begin
24     A=0;
25     B=0;
26     #5;
27
28     A=0;
29     B=1;
30     #5;
31
32
```

INFO:ProjectMgmt - Parsing design hierarchy completed successfully.

Started : "Launching ISE Text Editor to edit test_simulacija.v".



Design

View: Implementation Simulation

Behavioral

Hierarchy

- Simulacija_IO
 - xc3s1200e-5fg320
 - Logicko_kolo_Logicko_kolo_sch_tb

No Processes Running

No single design module is selected.

Design Utilities

```
13
14 // Bidirs
15
16 // Instantiate the UUT
17   Logicko_kolo UUT (
18     .A(A),
19     .B(B),
20     .Y(Y)
21   );
22 // Initialize Inputs
23 initial begin
24   A=0;
25   B=0;
26   #5;
27
28   A=0;
29   B=1;
30   #5;
31
32   A=1;
33   B=0;
34   #5;
35
36   A=1;
37   B=1;
38   #5;
39
40
```

INFO:ProjectMgmt - Parsing design hierarchy completed successfully.

Started : "Launching ISE Text Editor to edit test_simulacija.v".

Dupli Klik na Behavioral Check Syntax

The screenshot displays the Xilinx ISE Project Navigator interface. The main window shows a Verilog code file named `test_simulacija.v`. The code defines a module `Logicko_kolo` with inputs `A` and `B`, and output `Y`. It includes an `initial` block for setting initial values and a `behavioral` block for logic simulation. The code is as follows:

```
17   Logicko_kolo UUT (  
18       .A(A),  
19       .B(B),  
20       .Y(Y)  
21   );  
22   // Initialize Inputs  
23  
24   initial begin  
25       A=0;  
26       B=0;  
27       #5;  
28  
29       A=0;  
30       B=1;  
31       #5;  
32  
33       A=1;  
34       B=0;  
35       #5;  
36  
37       A=1;  
38       B=1;  
39       #5;  
40  
41   end  
42  
43  
44   endmodule
```

The left-hand side of the interface shows the Design Hierarchy tree, where the `UUT - Logicko_kolo` component is selected. Below the hierarchy, the Processes window shows the `Behavioral Check Syntax` process completed successfully. The Console window at the bottom displays the following messages:

```
ISim simulation engine GUI launched successfully  
  
Process "Simulate Behavioral Model" completed successfully
```

The status bar at the bottom indicates the current position is `Ln 40 Col 3` in the `Verilog` file.

Svako stanje definisali smo da traje 5 ciklusa, 5ns, #5
Dupli klik na Simulate Behavioral Model I pokrecemo ISim

The screenshot displays the ISE Project Navigator interface. The main window shows a Verilog code editor with the following code:

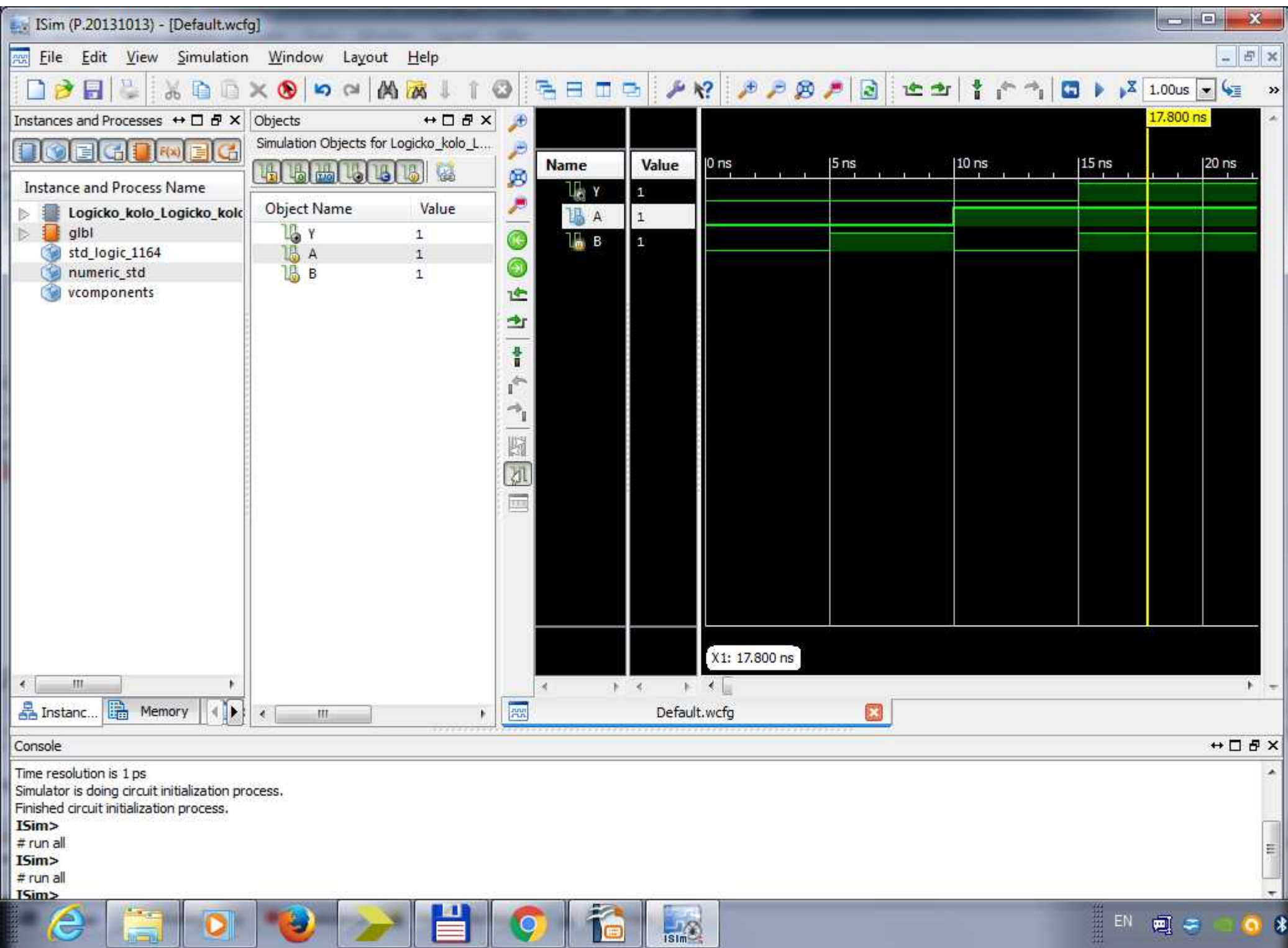
```
17   Logicko_kolo UUT (  
18       .A (A),  
19       .B (B),  
20       .Y (Y)  
21   );  
22   // Initialize Inputs  
23  
24   initial begin  
25       A=0;  
26       B=0;  
27       #5;  
28  
29       A=0;  
30       B=1;  
31       #5;  
32  
33       A=1;  
34       B=0;  
35       #5;  
36  
37       A=1;  
38       B=1;  
39       #5;  
40  
41   end  
42  
43  
44   endmodule
```

The left sidebar shows the Design view with the Simulation tab selected. The Hierarchy pane shows the project structure, including the file 'UUT - Logicko_kolo (Logicko_kolo.v)'. The Processes pane shows the 'Simulate Behavioral Model' process selected.

The Console window at the bottom displays the following output:

```
ISim simulation engine GUI launched successfully  
  
Process "Simulate Behavioral Model" completed successfully
```

The status bar at the bottom right indicates 'Ln 40 Col 3 Verilog'.



Na zoom zumiramo ulazne signale I pomeranjem klizaca pratimo stanja

The screenshot shows the Xilinx ISE simulation environment. The main window displays a logic simulator with a zoomed-in signal trace. The trace shows three signals, Y, A, and B, all of which are high (1) at the time shown. The time scale is 1.00us, and the zoomed-in view is labeled "Zoom to Full View" with a time range from 999,997 ps to 1,000,000 ps. The console window at the bottom shows a warning message: "WARNING: A WEBPACK license was found. WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license. WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version. This is a Lite version of ISim. Time resolution is 1 ps. Simulator is doing circuit initialization process. Finished circuit initialization process. ISim>".

Instances and Processes

- Logicko_kolo_Logicko_kolo
- gbl
- std_logic_1164
- numeric_std
- vcomponents

Objects

Simulation Objects for Logicko_kolo_L...

Name	Value
Y	1
A	1
B	1

Object Name Value

Object Name	Value
Y	1
A	1
B	1

Zoom to Full View

1,000,000 ps

999,997 ps 999,998 ps 999,999 ps 1,000,000 ps

X1: 1,000,000 ps

Default.wcfg

Console

WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>

Ln 40 Col 3 Verilog

8:16 PM
3/11/2016

ISE Project Navigator (P.20131013) - [Default.wcfg]

File Edit View Simulation Window Layout Help

Instances and Processes Objects

Simulation Objects for Logicko_kolo_L...

Instance and Process Name	Object Name	Value
Logicko_kolo_Logicko_kolo		
glibl		
std_logic_1164	Y	1
numeric_std	A	1
vcomponents	B	1

Name	Value
Y	0
A	0
B	0

0.000 ns

0 ns 20 ns 40 ns 60 ns 80 ns

X1: 0.000 ns

Default.wcfg

Console

WARNING: A WEBPACK license was found.
 WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
 WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
 This is a Lite version of ISim.
 Time resolution is 1 ps
 Simulator is doing circuit initialization process.
 Finished circuit initialization process.
 ISim>

